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Use of composite complementary-symmetry transistors in precise linear power amplification

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USE OF COMPOSITE COMPLEMENTARY-SYMMETRY TRANSISTORS IN PRECISE LINEAR POWER AMPLIFICATION

by

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INTRODUCTION

The performance of conventional linear power amplifiers has been limited either by the output transformer in the case of vacuum-tube amplifiers or by the characteristics of available transistors in the case of transistor amplifiers. Attempts to improve the performance of vacuum-tube amplifiers by the elimination of the output transformer have resulted in bulky and rather impractical amplifiers. The complementary-symmetry circuit proposed by Sziklai (17) in 1953 appears to offer great advantages in the design of linear power amplifiers, but power transistors which are suitable for use in this circuit are not available. The development of composite transistors which are extremely well suited for use in a complementary-symmetry output stage is shown to offer a good solution to this problem. The composite transistors, which have almost ideal characteristics, are composed of two readily-available transistors and associated circuitry. The design of an amplifier utilizing the composite transistors in a complementary-symmetry circuit is used to demonstrate the merits of this approach.

REVIEW OF CURRENT TECHNIQUES

In 1947, D. T. N. Williamson published an article which described the "Design for a High-Quality Amplifier" (18), and in 1949 he described a slightly improved version (19). The "Williamson Amplifier" as it has come to be known, was the standard of the industry for over a decade. The performance of the Williamson Amplifier has been exceeded in recent years by several vacuum-tube linear-amplifier designs but never by a significant margin. In his original article, Williamson outlines the basic principles of linear power amplification and the reasons that high-quality linear power amplification is required. In the most general terms, linear power amplification can be defined as supplying relatively large amounts of electrical power to a load impedance such that either the voltage or the current in the load is directly proportional to the input voltage or current and such that relatively little power is required from the input source. The most conventional type of amplifier is designed to produce an output voltage which is proportional to the input voltage and which will deliver between 10 and 100 watts into a 4 to 16 ohm resistive load for 1 volt input into 100,000 ohms (i.e., about 10^{-5} watts power input).

The criteria for the performance of a linear amplifier are usually given as: 1, the amount of non-linear distortion (harmonic and intermodulation) at various frequencies and

power levels; 2, the small-signal frequency response; 3, the power response for some arbitrarily set harmonic distortion, perhaps 1%; 4, the phase shift in the operating-frequency range; 5, the transient response; and 6, the output impedance. All of the active devices which are available for power amplification are non-linear devices and are incapable of satisfactorily meeting the above performance criteria when used in open-loop amplification. Williamson has shown that negative voltage feedback can be used to improve the performance of the basic active device in all of the above criteria. His final design utilizes 20 db of negative feedback to achieve 20 watts of power over a frequency range of 20 to 20,000 cps with less than 0.1% harmonic distortion. The low-level frequency response is within $\pm$ 1 db from 10 to 100,000 cps. The present state of the art is not significantly different from the original Williamson amplifier. The commercially available Harmon-Kardon Citation II, for example, has been acclaimed as the ultimate in power amplification. It utilizes 30 db of negative feedback to deliver 60 watts of power at 0.5% harmonic distortion over a frequency range of 20 to 20,000 cps. The low-level frequency response is within $\pm$ 1 db from 2 to 80,000 cps.

Significant improvements in vacuum-tube power-amplifier design will not be possible without a significant breakthrough in the design of the output transformer. Since vacuum tubes are generally low-current, high-voltage (i.e., high-impedance)

devices, it is necessary to use a transformer to match the output tubes to the low-impedance load. There have been some notable exceptions to this rule, but all have resulted in bulky and rather impractical amplifiers (4, 3). The low-frequency response of a transformer is limited by the primary inductance and results in a 6 db/octave gain reduction at low frequencies and the accompanying 90 degrees phase lead. The high-frequency response of a transformer is limited by the leakage inductance and distributed capacitance of the windings and ideally results in a 12 db/octave gain reduction at high frequencies with the accompanying 180 degrees phase lag. Even with this idealized model of a transformer, it is difficult to design an effective feedback circuit in a practical amplifier. The 180 degree phase shift at high frequencies can cause a zero degree phase margin even if the phase shift due to the remainder of the amplifier is neglected. And the designer of a vacuum-tube power amplifier soon finds that this idealized model of a transformer is not a good model. Multiple resonances that exist among the various windings of actual transformers result in a ragged response above the upper cutoff frequency. Thus virtually all of the compensation used to stabilize the amplifier must be accomplished below the upper-cutoff frequency of the output transformer. Likewise, the designer must beware of instability at the low frequencies. Nearly all vacuum-tube amplifiers require one and sometimes two coupling capacitors between the feedback point and the

output transformer. Each of the coupling capacitors contributes 90 degrees phase lead in addition to the 90 degrees phase lead inherent in the transformer. Thus zero phase margin and instability can result at the low frequencies unless the designer is careful to properly compensate for this effect.

The design of a transformer is a compromise between high primary inductance, low leakage inductance and low winding capacitance. High primary inductance requires a large high-permeability core and many turns in the primary winding. However, the larger the winding and the greater the number of turns, the greater will be the leakage inductance and winding capacitance. The principal reason that the Williamson amplifier has not been greatly improved in fifteen years is that better transformers have not become available. It appears that a great amount of work has gone into the design of the transformers which are currently available and it is doubtful that significantly better transformers will be available in the future.

The power transistor is the only other readily-available device which is capable of performing linear power amplification over a wide range of frequencies. The first transistors capable of dissipating reasonably large amounts of power were introduced less than a decade ago. Since that time an amazingly large number of power transistors have become available, some of them capable of dissipating as much as 170 watts and handling up to 25 amperes of collector current. Since the

transistor is capable of handling relatively high currents and must operate at relatively low voltages, it is ideally suited to be used in direct connection to the low-impedance loads which are traditionally used with power amplifiers. The designers of power amplifiers were quick to recognize some of the advantages of the power transistor and have published a great deal of different designs using this device. Some of the most outstanding advantages of the power transistor are its small size, light weight, and high electrical efficiency. Thus in applications such as mobile, public-address work where electrical efficiency and size are of prime importance, the advantages of the transistor outweigh all other considerations. In such applications the quality of the amplification is not of prime importance and very little thought has been given to this aspect of the design.

A great number of designs of transistor linear power amplifiers have also been published in which the avowed purpose of the design was high-quality, linear-power amplification (12, 7, 1). These were generally intended for use in high-fidelity audio systems. Many of the early designs incorporated a transformer either in the driver stage or in the output stage or in both. Since the transformer is the basic limiting factor in the performance of the vacuum-tube amplifier, one would expect that the use of a transformer in a transistor amplifier would establish a similar upper limit to its performance. This is in fact the case but one finds that this

limitation is even greater in a transistor amplifier because the power transistor itself has an inherent cutoff frequency due to the base charging capacitance and the input resistance which is usually below the cutoff frequency of a good transformer. These designs may serve as a satisfactory replacement for their vacuum-tube counterparts where the advantages of the transistor outweigh the inevitable reduction in performance. In transistor circuits the transformer is not required for impedance matching but is used so that two transistors of the same polarity can be operated in a symmetrical, push-pull mode. In 1953, Sziklai discussed the unique symmetrical properties of transistors, and showed that if enantiomorphic n-p-n and p-n-p transistors were available they could be used in a complementary fashion to achieve push-pull operation without the use of a coupling transformer (17). The advantages of complementary symmetry are very attractive since it permits the elimination of the output transformer, permits direct-coupling to the load, and has an inherent balance of bias level not present in single-ended design. Complementary symmetry has not been used for high-power amplification because enantiomorphic power transistors have not been available. Germanium power transistors of the p-n-p type have been available in the largest quantities and at the most reasonable prices, but only recently have there been germanium power transistors of the n-p-n type which could be used complementary to these p-n-p transistors. The n-p-n-germanium units which

are presently available have a very low cutoff frequency and are difficult to match to the p-n-p units. Silicon power transistors of the n-p-n type are also available but are generally much more costly than the germanium units and have no enantiomorphic counterpart.

A number of designs have used pseudo-complementary symmetry in which it is recognized that a p-n-p transistor operated in the common collector configuration behaves complementary to an identical p-n-p transistor in the common emitter configuration. There is an obvious loss of symmetry in this configuration, but the resulting distortion is usually reduced by over-all feedback (10, 6, 14).

THE COMPOSITE TRANSISTORS

Because the complementary-symmetry circuits of Sziklai offer many advantages to the designer of an extremely precise linear power amplifier, it is desirable to develop techniques to circumvent the problems that arise due to the lack of suitable power transistors. Figure 1 shows the basic complementary-symmetry circuit of Sziklai in which the common-emitter configuration is used in the output stage (17). This circuit may be modified as shown in Figure 2 so that the driver-output stage combination forms a direct-coupled group with no inherent d-c unbalance, quiescent voltage levels at the ground potential, and push-pull operation without the need for an output transformer. Impedances connected in boxes 1 and 2 can be used to provide a very versatile local feedback. The use of this circuit is limited by the non-availability of suitable transistors in the output stage. The purpose of this chapter is to describe the development of complementary-symmetry composite transistors which have characteristics much more suitable to use in this circuit than any available single transistor.

The N-p-n Composite Transistor

A p-n-p transistor in the common-collector configuration when driven by a current source behaves very much like an n-p-n transistor in the common-emitter configuration when driven by a current source. Thus the two transistors shown in Figure 3a

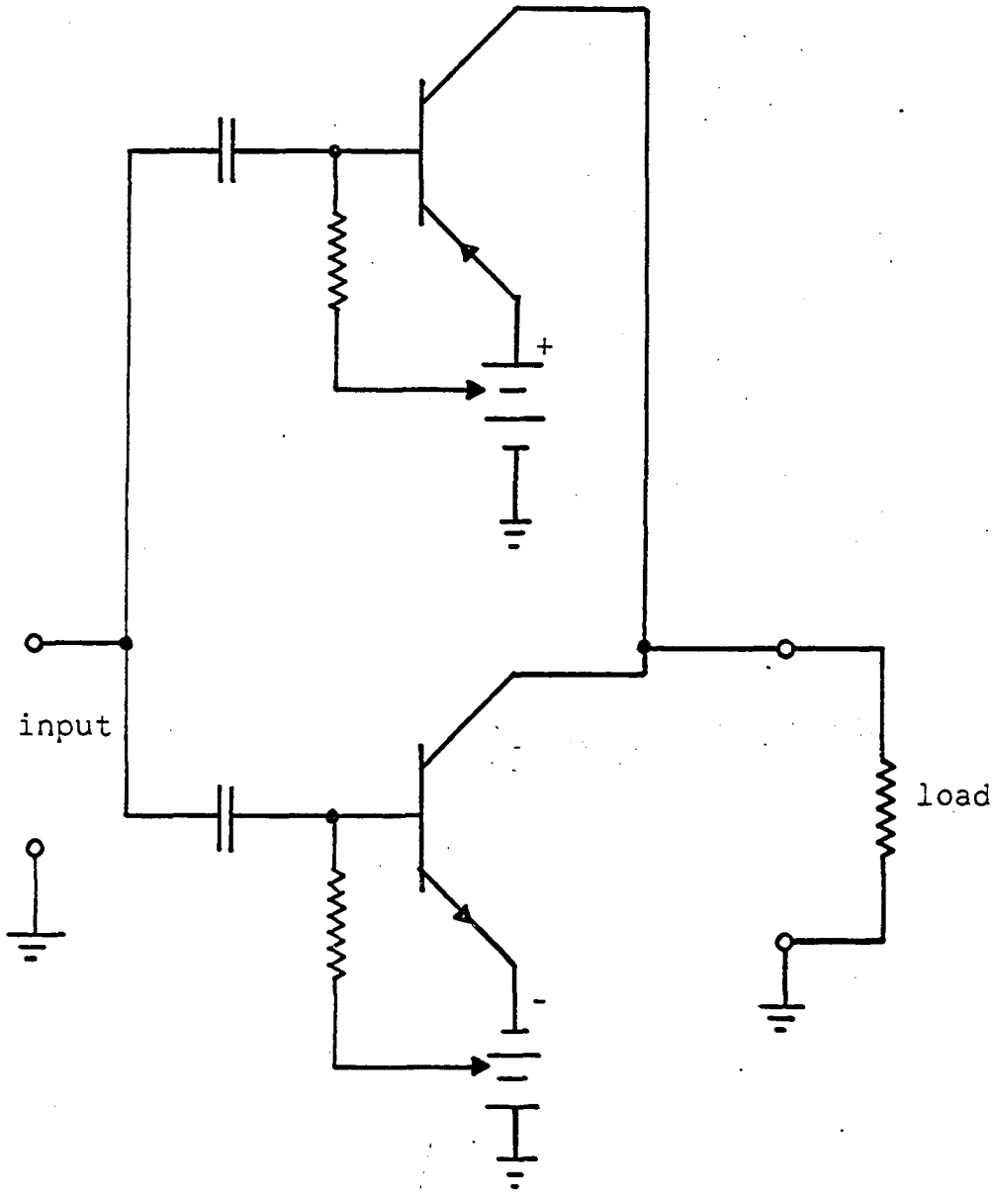


Figure 1. The basic complementary-symmetry circuit of Sziklai

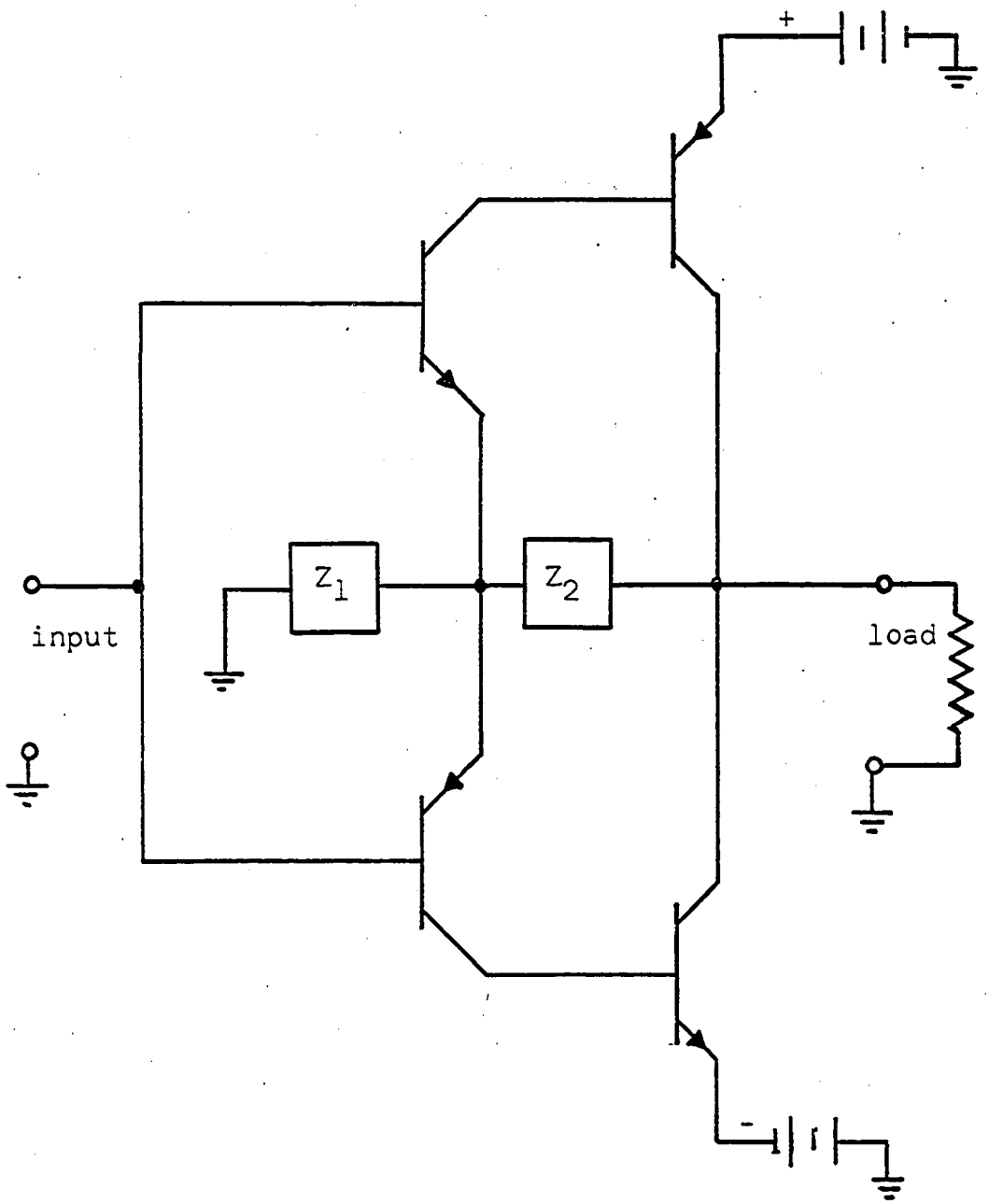


Figure 2. A modified form of complementary-symmetry circuit

behave somewhat like a single n-p-n power transistor. This composite transistor has the advantage that the power is largely dissipated by the p-n-p power transistor and a much smaller and readily-available n-p-n unit can be used in the driver stage. It has the disadvantage that the current gain and cutoff frequency are first order functions of the current gains and cutoff frequencies of the individual transistors. Any attempt to match such a composite transistor to an enantiomorphic counterpart would at best be a very tedious process and as a practical matter would probably be impossible. The addition of two impedances as shown in Figure 3b provides local series feedback and results in a composite n-p-n transistor whose characteristics are almost independent of the characteristics of the individual transistors as will be shown by the following analysis. If the bias levels are ignored for the present, the composite transistor of Figure 3b may be represented for small-signal purposes by the set of two-port networks shown in Figure 4a. Note the addition of a current-source input and a load to complete the circuit as it will appear in the final form. In the analysis, a two-port network will be represented by a matrix using the standard notation as given by Shea (16). The subscript will indicate the particular element of a matrix and the superscript will indicate the matrix to which it belongs. Thus b_{12}^{iv} will be the first-row, second-column element of the B matrix for the fourth two-port network. The hybrid-π model of the transistor will

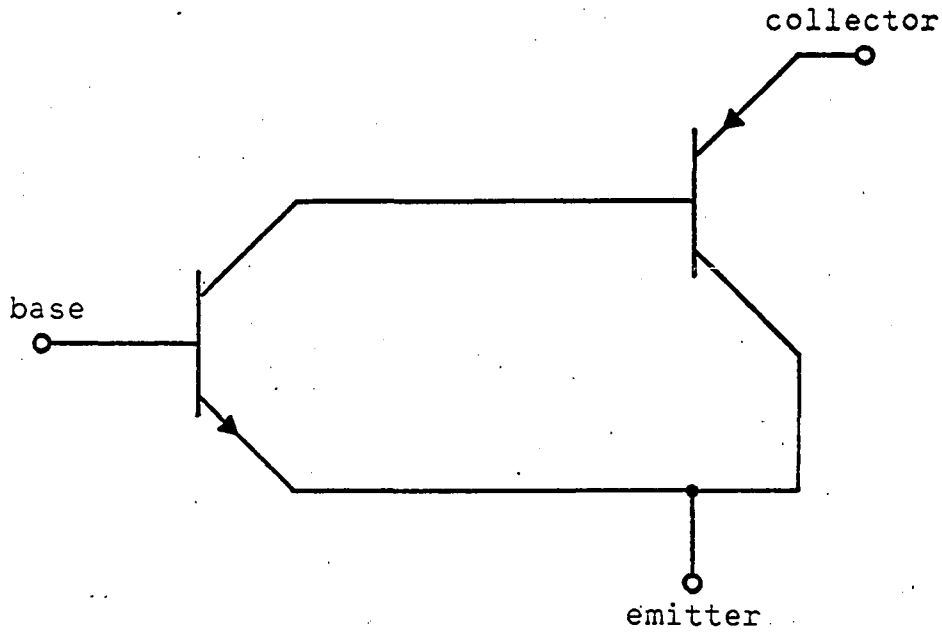


Figure 3a. One possible composite n-p-n transistor

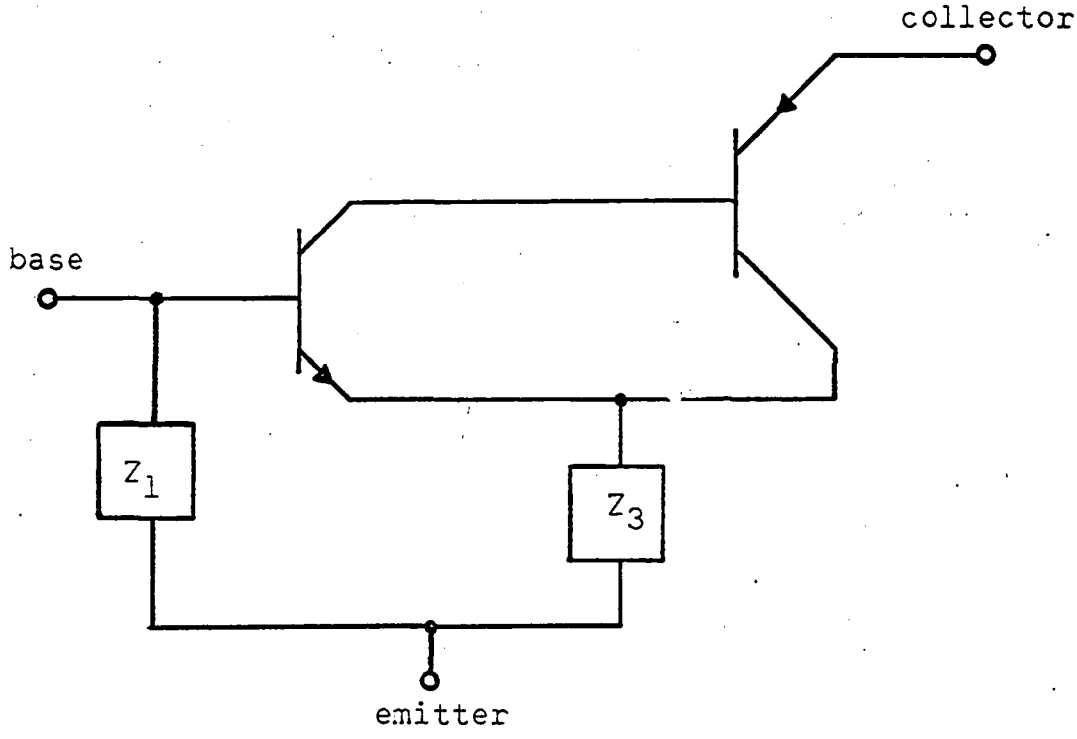


Figure 3b. The final form of the composite n-p-n transistor

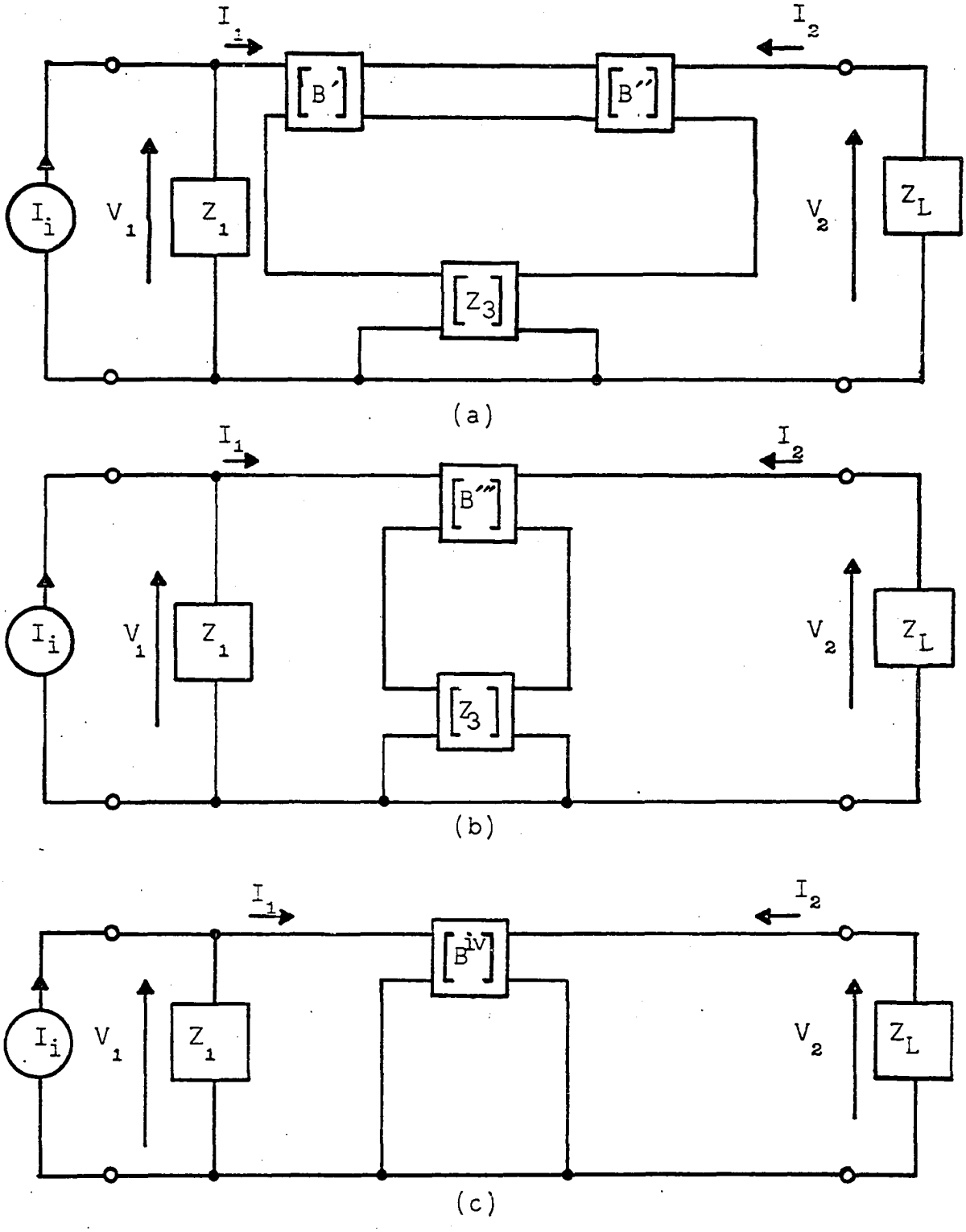


Figure 4. Sequence of two-port networks used in the analysis of the n-p-n composite transistor

be used as the standard model for all of the following analysis (15). This model represents the transistor quite satisfactorily for small-signal analysis below the α-cutoff frequency and its parameters are readily interpreted as physical quantities. The approximate h-parameters as derived from the hybrid-π model are given in the Appendix and will be used as a starting point for this analysis. Converting the h-parameters to b-parameters by standard conversion methods, the matrices become

$$[B'] = \begin{bmatrix} \dfrac{Z'_\mu}{Z'_\pi} & \dfrac{Z'_\mu}{Z'_\pi}(R'_x + Z'_\pi) \\ \dfrac{Z'_\mu}{r'_o Z'_\pi} + \dfrac{h'_{fe}}{Z'_\pi} & \dfrac{Z'_\mu}{r'_o Z'_\pi}(R'_x + Z'_\pi) + \dfrac{R'_x h'_{fe}}{Z'_\pi} \end{bmatrix} \qquad (1)$$

and

$$[B''] = \begin{bmatrix} \dfrac{1}{r''_o} + \dfrac{h''_{fe}}{Z''_\mu} & R''_x + Z''_\pi \\ & 1 + h''_{fe} \end{bmatrix} \qquad (2)$$

Combining $[B']$ and $[B'']$ into $[B''']$ the diagram of Figure 4a becomes that of 4b. Terms which are smaller by about two orders of magnitude or more with respect to other terms in a sum will be neglected. Thus $[B''']$ becomes,

$$[B'''] = \begin{bmatrix} \dfrac{Z'_\mu}{Z'_\pi} & \\ \dfrac{(1 + h''_{fe})Z'_\mu}{r'_o Z'_\pi} + \dfrac{(1 + h''_{fe})h'_{fe}}{Z'_\pi} & \end{bmatrix}$$

(second column of $[B''']$ on next page)

$$\frac{Z'_\mu}{Z'_\pi}(R'_x + Z'_\pi)$$

$$(1 + h''_{fe}) \quad \frac{Z'_\mu (R'_x + Z'_\pi)}{r'_o Z'_\pi} + (1 + h''_{fe})h'_{fe} \quad \frac{R'_x}{Z'_\pi}\Bigg] \tag{3}$$

or converting to z-parameters,

$$[Z'''] = \begin{bmatrix} \dfrac{Z'_\mu (R'_x + Z'_\pi)}{Z'_\mu + h'_{fe}r'_o} + \dfrac{h'_{fe}R'_x r'_o}{Z'_\mu + h'_{fe}r'_o} & \dfrac{Z'_\pi r'_o}{(1+h''_{fe})(Z'_\mu + h'_{fe}r'_o)} \\ - \dfrac{Z'_\mu r'_o h'_{fe}}{Z'_\mu + h'_{fe}r'_o} & \dfrac{Z'_\mu r'_o}{(1+h''_{fe})(Z'_\mu + h'_{fe}r'_o)} \end{bmatrix}. \tag{4}$$

Combining $[Z''']$ and $[Z_3]$, the diagram of Figure 4b becomes Figure 4c, and

$$[Z^{iv}] = \frac{1}{Z'_\mu + h'_{fe}r'_o} \begin{bmatrix} Z'_\mu(R'_x + Z'_\pi) + h'_{fe}R'_x r'_o & \dfrac{Z'_\pi r'_o}{1+h''_{fe}} + Z_3 Z'_\mu + Z_3 h'_{fe} r'_o \\ - Z'_\mu r'_o h'_{fe} & \dfrac{Z'_\mu r'_o}{1+h''_{fe}} \end{bmatrix}. \tag{5}$$

Note that

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z^{iv}] \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{6}$$

or

$$\begin{bmatrix} V_1 \\ \\ Z_L I_2 \end{bmatrix} = \begin{bmatrix} Z^{iv} \end{bmatrix} \begin{bmatrix} I_i - \frac{V_1}{Z_1} \\ \\ I_2 \end{bmatrix} . \qquad (7)$$

Solving these equations for I_2,

$$I_2 = \frac{\begin{vmatrix} 1 + \frac{Z_{11}^{iv}}{Z_1} & Z_{11}^{iv} I_i \\ \frac{Z_{21}^{iv}}{Z_1} & Z_{21}^{iv} I_i \end{vmatrix}}{\begin{vmatrix} 1 + Z_{11}^{iv} & -Z_{12}^{iv} \\ \frac{Z_{21}^{iv}}{Z_1} & -(Z_L + Z_{22}^{iv}) \end{vmatrix}} \qquad (8)$$

$$I_2 \approx - \frac{Z_{21}^{iv} I_i}{(1 + \frac{Z_{11}^{iv}}{Z_1}) Z_{22}^{iv} - \frac{Z_{12}^{iv} Z_{21}^{iv}}{Z_1}} . \qquad (9)$$

Substituting values for the $[Z^{iv}]$ elements,

$$\frac{I_2}{I_i} = \frac{h_{fe}'(1 + h_{fe}'')}{1 + \frac{R_x' + Z_\pi'}{Z_1} + \frac{Z_3 h_{fe}'(1 + h_{fe}'')}{Z_1}} . \qquad (10)$$

Before considering this equation further, the equations for a p-n-p composite transistor will be derived.

The P-n-p Composite Transistor

The p-n-p composite transistor is a variation of the Darlington composite transistor incorporating the addition of series feedback. The basic circuit is shown in Figure 5. Again ignoring the bias levels for the moment, the equivalent circuit may be represented as in Figure 6a. Using the hybrid-π parameters given in Appendix I and converting to z-parameters:

$$[Z'''] = \frac{1}{\frac{1}{r_o'''} + \frac{h_{fe}'''}{Z_\mu'''}} \begin{bmatrix} \frac{R_x''' + Z_\pi'''}{r_o'''} + \frac{R_x''' h_{fe}'''}{Z_\mu'''} & \frac{Z_\pi'''}{Z_\mu'''} \\ -h_{fe}''' & 1 \end{bmatrix} \qquad (11)$$

By combining $[Z''']$ with $[Z_3]$, Figure 6a becomes Figure 6b and

$$[Z^{iv}] = \frac{1}{\frac{1}{r_o'''} + \frac{h_{fe}'''}{Z_\mu'''}} \begin{bmatrix} \frac{R_x''' + Z_\pi'''}{r_o'''} + \frac{R_x''' h_{fe}'''}{Z_\mu'''} + \frac{Z_3}{r_o'''} + \frac{Z_3 h_{fe}'''}{Z_\mu'''} & \frac{Z_\pi'''}{Z_\mu'''} + \frac{Z_3}{r_o'''} + \frac{Z_3 h_{fe}'''}{Z_\mu'''} \\ -h_{fe}''' & 1 \end{bmatrix} \qquad (12)$$

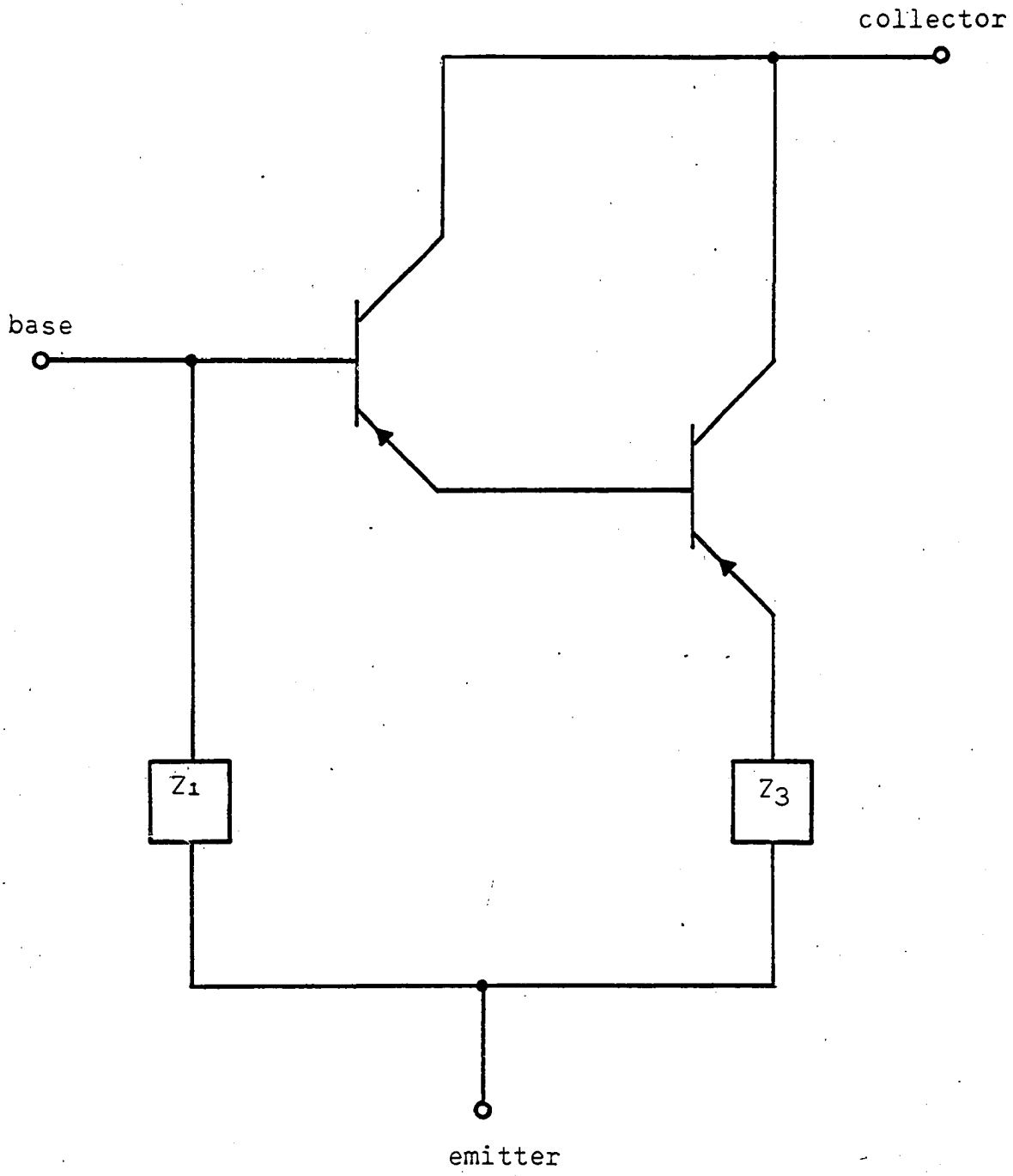


Figure 5. The p-n-p composite transistor

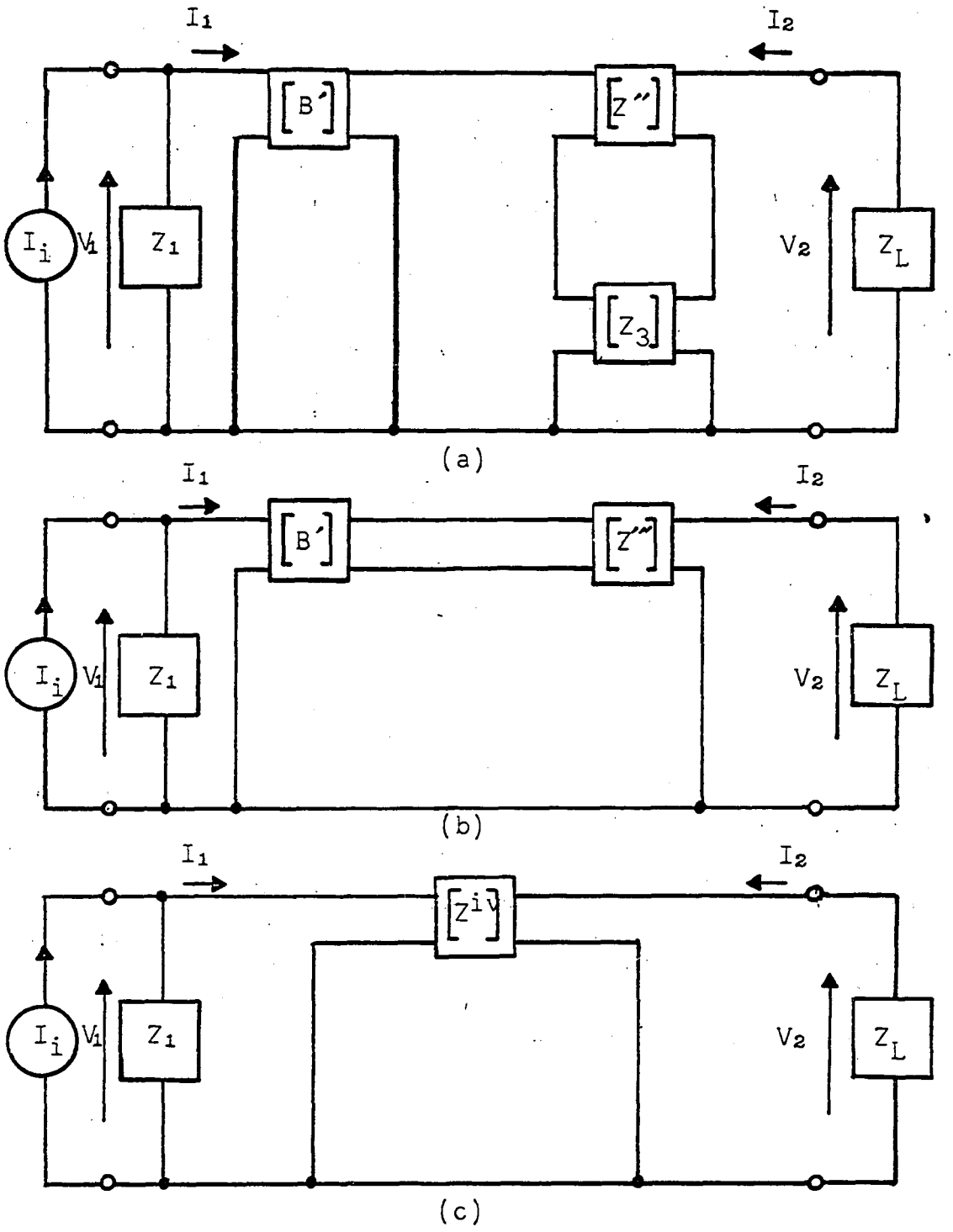


Figure 6. Sequence of two-port networks used in the analysis of the p-n-p composite transistor

Now

$$[B'] = \begin{bmatrix} 1 & R_x' + Z_\pi' \\ \frac{1}{r_o'} + \frac{h_{fe}'}{Z_\mu'} & 1 + h_{fe}' \end{bmatrix} . \qquad (13)$$

Combining $[B']$ and $[Z'']$, Figure 6b becomes Figure 6c where

$$[B^{iv}] = \frac{1}{\frac{Z_\pi''}{Z_\mu''} + \frac{Z_3}{r_o''} + \frac{Z_3 h_{fe}''}{Z_\mu''}} \begin{bmatrix} 1 & \\ \frac{1}{r_o''} + \frac{h_{fe}''}{Z_\mu''} & \end{bmatrix}$$

$$\begin{bmatrix} R_x' + Z_\pi' + (1+h_{fe}')(R_x'' + Z_\pi'' + h_{fe}'' Z_3) & \\ (R_x' + Z_\pi')\left[\frac{1}{r_o''} + \frac{h_{fe}''}{Z_\mu''}\right] + (1 + h_{fe}')\left[\frac{R_x''+Z_\pi''+Z_3}{r_o''}\right. & \\ \left. + \frac{(R_x'' + Z_3)h_{fe}''}{Z_\mu''}\right] & \end{bmatrix} \qquad (14)$$

or

$$[Z^{iv}] = \left(\frac{1}{\frac{1}{r_o''} + \frac{h_{fe}''}{Z_\mu''}} \right) \text{(remainder of matrix on page 22)}$$

$$\begin{bmatrix} (R_x' + Z_\pi')\left(\frac{1}{r_o''} + \frac{h_{fe}''}{Z_\mu''}\right) + (1 + h_{fe}')\left(\frac{R_x'' + Z_\pi'' + Z_3}{r_o''} + \frac{(R_x'' + Z_3)h_{fe}''}{Z_\mu''}\right) & \frac{Z_\pi''}{Z_\mu''} + \frac{Z_3}{r_o''} + \frac{Z_3 h_{fe}''}{Z_\mu''} \\ -(1 + h_{fe}')h_{fe}'' & 1 \end{bmatrix} \quad (15)$$

From Equation 9,

$$\frac{I_2}{I_i} = \frac{(1 + h_{fe}')h_{fe}''}{1 + \frac{R_x' + Z_\pi'}{Z_1} + \frac{(1 + h_{fe}')(R_x'' + Z_\pi'' + Z_3)}{Z_1} + \frac{(1 + h_{fe}')h_{fe}''Z_3}{Z_1}} \quad (16)$$

The Selection of Z_1 and Z_3

Equation 10 for the n-p-n composite transistor and Equation 16 for the p-n-p composite are very similar and a proper choice of Z_1 and Z_3 can cause the undesirable terms to become insignificant. At low frequencies, $h_{fe} = \beta$ and $Z_1 = R_1$, $Z_3 = R_3$ since Z_1 and Z_3 cannot have a pole at the origin. Therefore,

$$\left(\frac{I_2}{I_i}\right)_{n\text{-}p\text{-}n} = \frac{\beta'(1+\beta'')}{1 + \frac{R_x' + R_\pi'}{R_1} + \frac{R_3}{R_1}\beta'(1+\beta'')} \tag{17}$$

and

$$\left(\frac{I_2}{I_i}\right)_{p\text{-}n\text{-}p} = \frac{(1+\beta')\beta''}{1 + \frac{R_x' + R_\pi'}{R_1} + (1+\beta')\frac{R_x'' + R_\pi'' + R_3}{R_1} + \frac{R_3(1+\beta')\beta''}{R_1}}. \tag{18}$$

Note that if R_1 and R_3 are chosen so that

$$1 + \frac{R_x' + R_\pi'}{R_1} \ll \frac{R_3}{R_1}\beta'(1+\beta'') \tag{19}$$

for the n-p-n composite transistor and

$$1 + \frac{R_x' + R_\pi'}{R_1} + \frac{(1+\beta')(R_x'' + R_\pi'' + R_3)}{R_1} \ll \frac{R_3(1+\beta')\beta''}{R_1} \tag{20}$$

for the p-n-p composite transistor, then Equation 17 and Equation 18 reduce to

$$\left(\frac{I_2}{I_i}\right)_{n\text{-}p\text{-}n} = \frac{R_1}{R_3} \tag{21}$$

and

$$\left(\frac{I_2}{I_i}\right)_{p\text{-}n\text{-}p} = \frac{R_1}{R_3}. \tag{22}$$

Under these conditions the current gains of the two composite transistors will be equal, constant, and virtually independent of operating point. To achieve these conditions it is necessary in the case of the p-n-p composite transistor that

$$\frac{(1 + \beta')(R_x'' + R_\pi'' + R_3)}{R_1} << \frac{R_3}{R_1}(1 + \beta')\beta'' \qquad (23)$$

$$R_x'' + R_\pi'' + R_3 << R_3\beta''. \qquad (24)$$

For the power transistors used in this project

$$R_x'' + R_\pi'' \approx 5 \text{ to } 20 \text{ ohms}$$

$$\beta'' \approx 75$$

Therefore, R_3 should be chosen between 0.5 and 5 ohms with the higher values yielding a better approximation to inequality 24. R_3 also determines the saturation resistance of the composite transistor and a high value of R_3 greatly reduces the power-handling capacity of the final amplifier. A value of 2.2 ohms was chosen for R_3 in the final design. Note also that

$$\frac{R_3}{R_1}\beta'(1 + \beta'') >> 1$$

or

$$R_1 << R_3\beta'(1 + \beta'') \approx 5000.$$

Since R_1/R_3 determines the current gain of the composite transistor, it is desirable to make R_1 as large as possible. However, the above inequality limits R_1 to be less than 500 ohms. A value of 250 ohms was chosen. This choice of R_1 and R_3 provides a composite transistor with a current gain of 250/2.2 = 114 which is essentially independent of individual

transistor characteristics and operating points.

High-Frequency Matching

It is desirable that the output transistors of a push-pull stage be matched not only for low frequency β but also for current gain well beyond the β cutoff frequency (5). The single pole approximation to h_{fe} is excellent for investigating the high frequency characteristics of these composite transistors (16). Thus

$$h_{fe} = \frac{\beta}{1 + j \frac{f}{f_\beta}} \tag{25}$$

and Equations 10 and 16 become

$$\frac{I_2}{I_i}_{n\text{-}p\text{-}n} = \frac{\frac{\beta'}{1 + j\frac{f}{f_{\beta'}}} \left(1 + \frac{\beta''}{1 + j\frac{f}{f_{\beta''}}}\right)}{1 + \frac{R'_x + Z'_\pi}{Z_1} + \frac{Z_3}{Z_1} \frac{\beta'}{1+j\frac{f}{f_{\beta'}}} \left(1 + \frac{\beta''}{1+j\frac{f}{f_{\beta''}}}\right)}$$

or to a good approximation

$$\frac{I_2}{I_i}_{n\text{-}p\text{-}n} = \frac{\beta'(1+\beta'')/(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}})}{1 + \frac{R'_x + Z'_\pi}{Z_1} + \frac{Z_3}{Z_1} \beta'(1+\beta'')/(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}})} \tag{26}$$

and

$$\frac{I_2}{I_i}_{p\text{-}n\text{-}p} = \frac{(1 + \frac{\beta'}{1+j\frac{f}{f_{\beta'}}})(\frac{\beta''}{1+j\frac{f}{f_{\beta''}}})}{1 + \frac{R_x'+Z_\pi'}{Z_1} + (1+\frac{\beta'}{1+j\frac{f}{f_{\beta'}}})\frac{R_x''+Z_\pi''+Z_3}{Z_1}}$$

$$\frac{}{+ (1 + \frac{\beta'}{1+j\frac{f}{f_{\beta'}}}) \frac{\beta''}{1+j\frac{f}{f_{\beta''}}} Z_3}$$

$$Z_1$$

or to a good approximation

$$\frac{I_2}{I_i}_{p\text{-}n\text{-}p} = \frac{\beta''(1+\beta')/(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}})}{1 + \frac{R_x' + Z_\pi'}{Z_1} + (1+\beta')\frac{R_x''+Z_\pi''+ Z_3}{(1+j\frac{f}{f_{\beta'}})Z_1} + \frac{(1+\beta')\beta'' Z_3}{(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}})Z_1}} \tag{27}$$

In order for these equations to represent similar current gains, the following inequality must hold:

$$R_x''+ Z_\pi'' + Z_3 << \frac{\beta'' Z_3}{1+j\frac{f}{f_{\beta''}}} \tag{28}$$

Since this is a weak inequality even at low frequencies, it can be maintained only by canceling the pole in the denominator of the right-hand side with a zero in Z_3. Thus Z_3 should have

the form,

$$Z_3 = R_3(1+j\frac{f}{f_{\beta''}}) = R_3(1+j\frac{2\pi fL}{R_3}) \qquad (29)$$

Assuming $f_{\beta''}$ to be in the order of 10^5 cps, this requires that

$$L = 2.2/2\pi \times 10^5 = 3.5 \text{ microhenries.}$$

By letting $Z_1 = R_1$, the following inequalities will now hold, for the p-n-p composite transistor,

$$1 + \frac{R_x' + Z_\pi'}{R_1} + \frac{(1+\beta')(R_x'' + Z_\pi'' + Z_3)}{(1+j\frac{f}{f_{\beta'}})R_1} << \frac{(1+\beta')\beta'' Z_3}{(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}})R_1}$$

and for the n-p-n composite transistor,

$$1 + \frac{R_x' + Z_\pi'}{R_1} << \frac{Z_3\beta'(1+\beta'')}{R_1}/(1+j\frac{f}{f_{\beta'}})(1+j\frac{f}{f_{\beta''}}).$$

Thus for both the p-n-p and n-p-n composite transistors,

$$\frac{I_2}{I_i} = \frac{R_1}{Z_3} = \frac{R_1}{R_3(1+j\frac{\omega L}{R_3})} \qquad (30)$$

Each composite transistor is an enantiomorphic counterpart of the other to the extent that the above are good approximations. With transistors which are readily available, it is possible to choose R_1, R_3, and L so that Equation 30 is valid to about 3 megacycles. Figures 7a and 7b show the diagrams of an n-p-n composite transistor and a p-n-p composite transistor based on the above findings. The bias

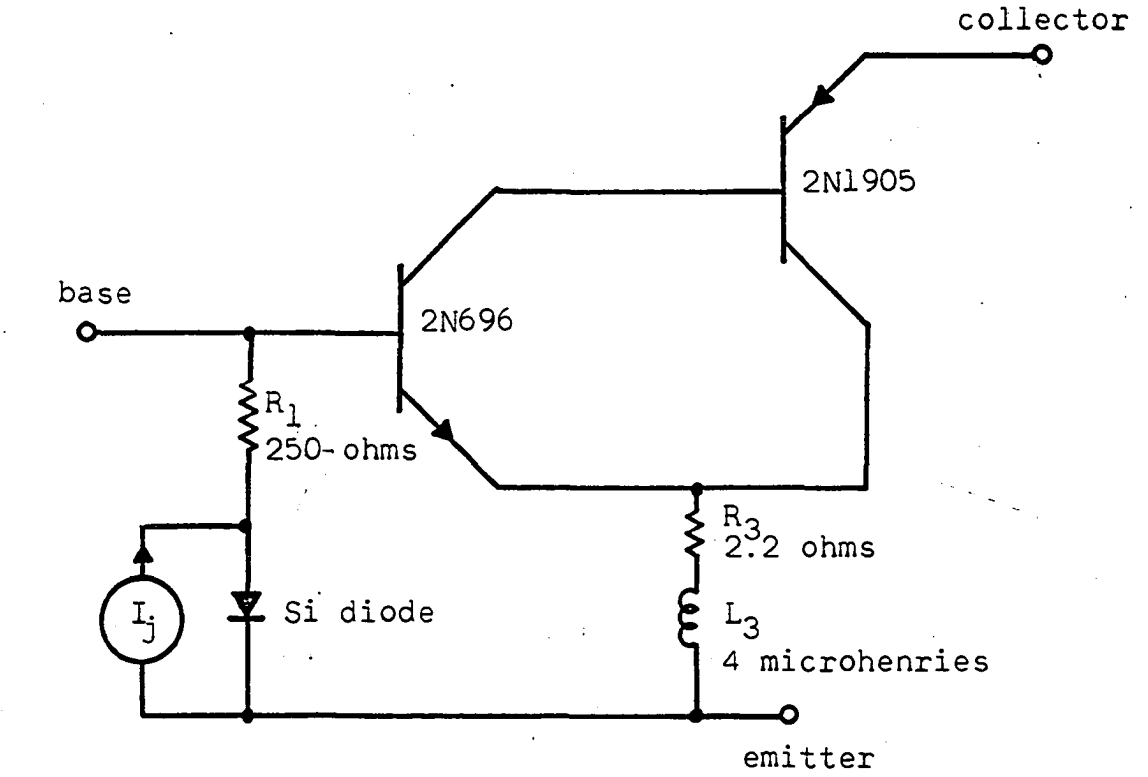


Figure 7a. The n-p-n composite transistor

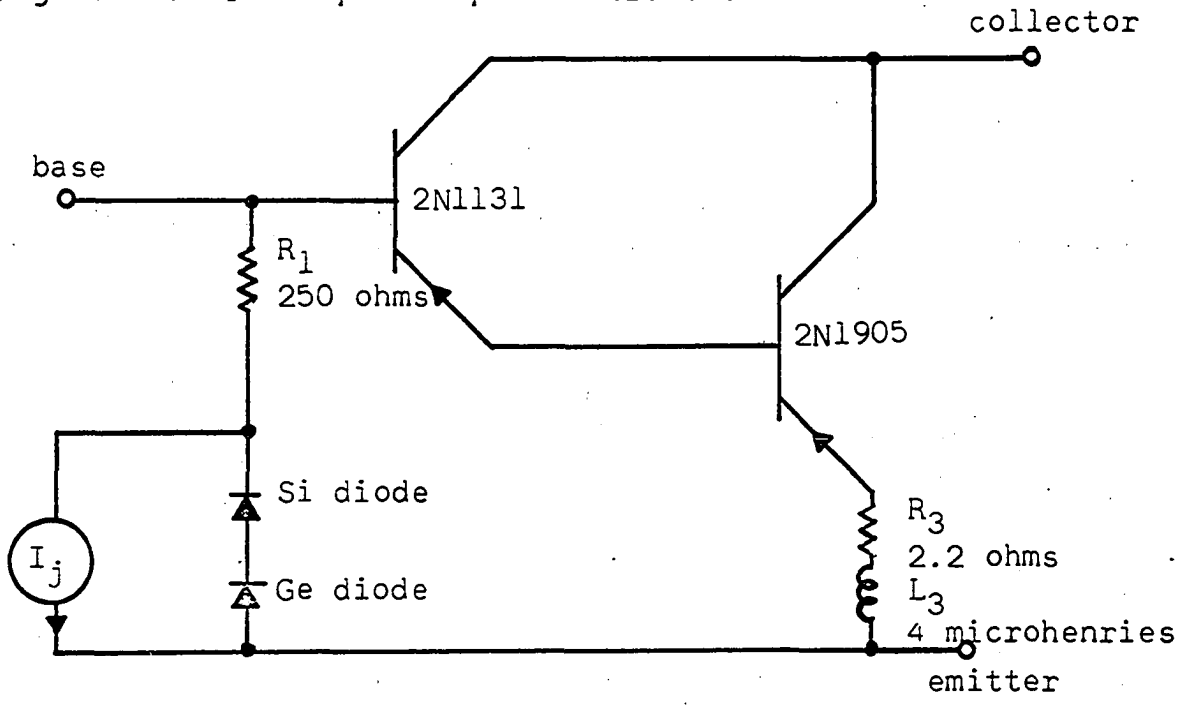
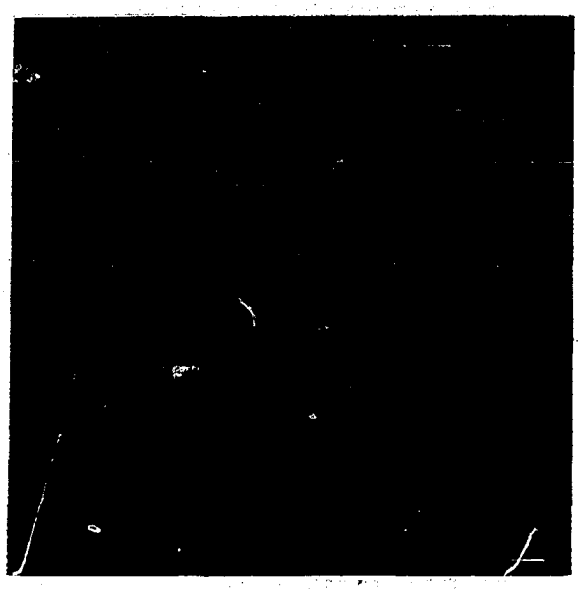


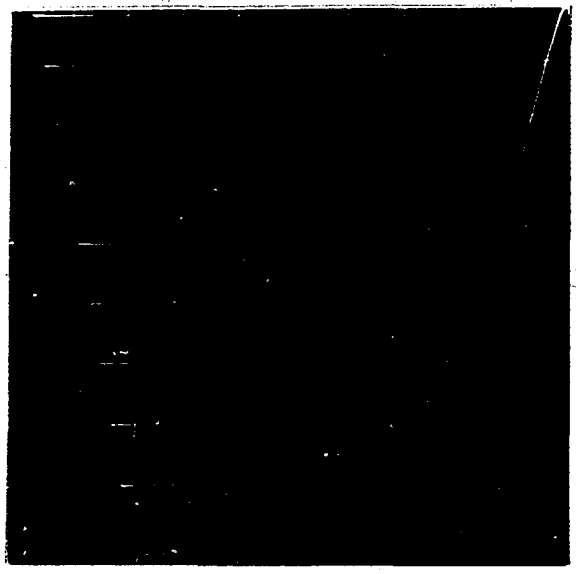
Figure 7b. The p-n-p composite transistor

levels are simply established across a diode junction of the same type as the emitter-base junction of the transistor in question. The junction of the diode can be forward biased by a current I_j so that each transistor has the same I_{ceo}. The collector curves of the composite transistors shown in Figure 8 demonstrate the validity of the low-frequency analysis.



Vertical sensitivity = 200 milliamperes/division
Horizontal sensitivity = 2 volts/division
Base current increment = 2 milliamperes/step

Figure 8a. Collector curves for the n-p-n composite transistor



Vertical sensitivity = 200 milliamperes/division
Horizontal sensitivity = 2 volts/division
Base current increment = 2 milliamperes/step

Figure 8b. Collector curves for the p-n-p composite transistor

THE OUTPUT AND DRIVER STAGES

With the design of the composite enantiomorphic transistors completed, one may now investigate the performance of the circuit of Figure 2 with the output transistors replaced by the composite transistors.

Choice of Class of Amplification

In any type of push-pull amplification, the designer must decide whether the class of amplification should be A, AB, or B. Class A amplification is attractive principally because it is effective in reducing inherent distortion in the output stage. Class A is particularly undesirable for transistor circuits since maximum collector dissipation occurs at quiescent conditions and heat sinks must be designed to dissipate this power continuously. Class B is particularly desirable in this respect since there is no collector dissipation in quiescent conditions. Also the higher theoretical efficiency of a class-B output stage is advantageous in reducing the collector dissipation at all signal levels (8). Bias stability is critical in class B amplification because a change in bias levels can cause a crossover dead zone in which neither transistor is conducting. This dead zone can cause great distortion at low-level signals. The total elimination of bias-level shift due to temperature changes is at best a tedious job of tailoring temperature-compensation networks to indivi-

dual transistors. In AB operation the bias level may be allowed to shift considerably without seriously affecting the performance of the amplifier. However, the transistors are essentially current sources driving a low-impedance load, and the part of the cycle in which both transistors are conducting will have twice the gain as will the remainder of the cycle. The output waveform of a class-AB transistor amplifier in response to a sine wave should have the form,

$$g(\omega t) = E_m \sin \omega t + f(\omega t)$$

where

$$f(\omega t) = E_m \sin \omega t \qquad -\pi \leq \omega t < -\pi + \mathrm{Sin}^{-1} \frac{E_1}{E_m}$$

$$= -E_1 \qquad -\pi + \mathrm{Sin}^{-1} \frac{E_1}{E_m} < \omega t < -\mathrm{Sin}^{-1} \frac{E_1}{E_m}$$

$$= E_m \sin \omega t \qquad -\mathrm{Sin}^{-1} \frac{E_1}{E_m} < \omega t < \mathrm{Sin}^{-1} \frac{E_1}{E_m}$$

$$= E_1 \qquad \mathrm{Sin}^{-1} \frac{E_1}{E_m} < \omega t < \pi - \mathrm{Sin}^{-1} \frac{E_1}{E_m}$$

$$= E_m \sin \omega t \qquad \pi - \mathrm{Sin}^{-1} \frac{E_1}{E_m} < \omega t \leq \pi$$

The Fourier components of $f(\omega t)$ are determined by

$$b_n = 0 \qquad n \text{ even}$$

$$b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\omega t) \sin n\omega t \, d\, \omega t \qquad n \text{ odd}$$

$$b_n = \frac{4}{\pi}\left[E_m \int_0^{\mathrm{Sin}^{-1}\frac{E_1}{E_m}} \sin\omega t \sin n\omega t \, d\,\omega t + E_1 \int_{\mathrm{Sin}^{-1}\frac{E_1}{E_m}}^{\pi/2} \sin n\omega t \, d\,\omega t\right]$$

n odd

$$b_1 = \frac{4}{\pi}\left[E_m \int_0^{\mathrm{Sin}^{-1}\frac{E_1}{E_m}} \sin^2\omega t \, d\,\omega t + E_1 \int_{\mathrm{Sin}^{-1}\frac{E_1}{E_m}}^{\pi/2} \sin\omega t \, d\,\omega t\right]$$

$$= \frac{2E_m}{\pi}\left[\mathrm{Sin}^{-1}\frac{E_1}{E_m} + \frac{E_1}{E_m}\sqrt{1 - \left[\frac{E_1}{E_m}\right]^2}\,\right]$$

Let b_1' be the Fourier component of $g(\omega t)$, then

$$b_1' = E_m + b_1 = E_m\left[1 + \frac{2}{\pi}\,\mathrm{Sin}^{-1}\frac{E_1}{E_m} + \frac{2}{\pi}\,\frac{E_1}{E_m}\sqrt{1 - \left[\frac{E_1}{E_m}\right]^2}\,\right]$$

$$b_3 = b_3' = \frac{4}{\pi}\left[E_m \int_0^{\mathrm{Sin}^{-1}\frac{E_1}{E_m}} \sin\omega t \sin 3\omega t \, d\,\omega t + E_1 \int_{\mathrm{Sin}^{-1}\frac{E_1}{E_m}}^{\pi/2} \sin 3\omega t \, d\omega t\right.$$

$$= \frac{4}{3}\,\frac{E_1}{\pi}\left[1 - \left[\frac{E_1}{E_m}\right]^2\right]^{3/2} .$$

The maximum third harmonic energy occurs when

$$\frac{db_3'}{dE_1} = 0 = \frac{4}{3\pi}\left[\frac{3}{2}\,E_1\left[1 - \left[\frac{E_1}{E_m}\right]^2\right]^{1/2}\left(-2\,\frac{E_1}{E_m^2}\right) + \left[1 - \left[\frac{E_1}{E_m}\right]^2\right]^{3/2}\right]$$

$$\frac{E_1}{E_m} = 1/2$$

Thus

$$b_{3\ max}' = 4/3\ \frac{E_1}{\pi}\left[1 - \left(\frac{1}{2}\right)^2\right]^{3/2} = 0.284\ E_1$$

and

$$b_1' \Big|_{\frac{E_1}{E_m} = 1/2} = 2E_1\left[1 + \frac{2}{\pi}\ \text{Sin}\ 1/2 + \frac{2}{\pi}\left(\frac{1}{2}\right)\left(\frac{3}{4}\right)^{1/2}\right]$$

$$= 3.216\ E_1$$

Thus the third-harmonic distortion when the third-harmonic energy is maximum is

$$\%\ b_3' = \frac{0.284\ E_1}{3.216\ E_1} \times 100 = 8.8\%$$

and this is a very good approximation to the maximum third-harmonic distortion. Because of the extreme linearity and balance that can be achieved with the composite transistors, this distortion is by far the greatest distortion encountered in the circuit under consideration. A measurement of the distortion in the circuit to be proposed revealed a maximum total harmonic distortion of 6%. This reduction in distortion from the theoretical maximum is due to the fact that the transistors do not have a sharp cutoff of gain at zero collector current, but rather a gradual reduction in gain as the collector current approaches zero. The 6% distortion is a relatively high inherent distortion, but the advantages gained in efficiency, power dissipation, and crossover distortion

dictate that class-AB operation must be chosen in high-quality transistor power amplification unless one is willing to accept the unnecessary complications of elaborate bias-stabilizing circuits or extremely large heat sinks.

Final Design of Output and Driver Stages

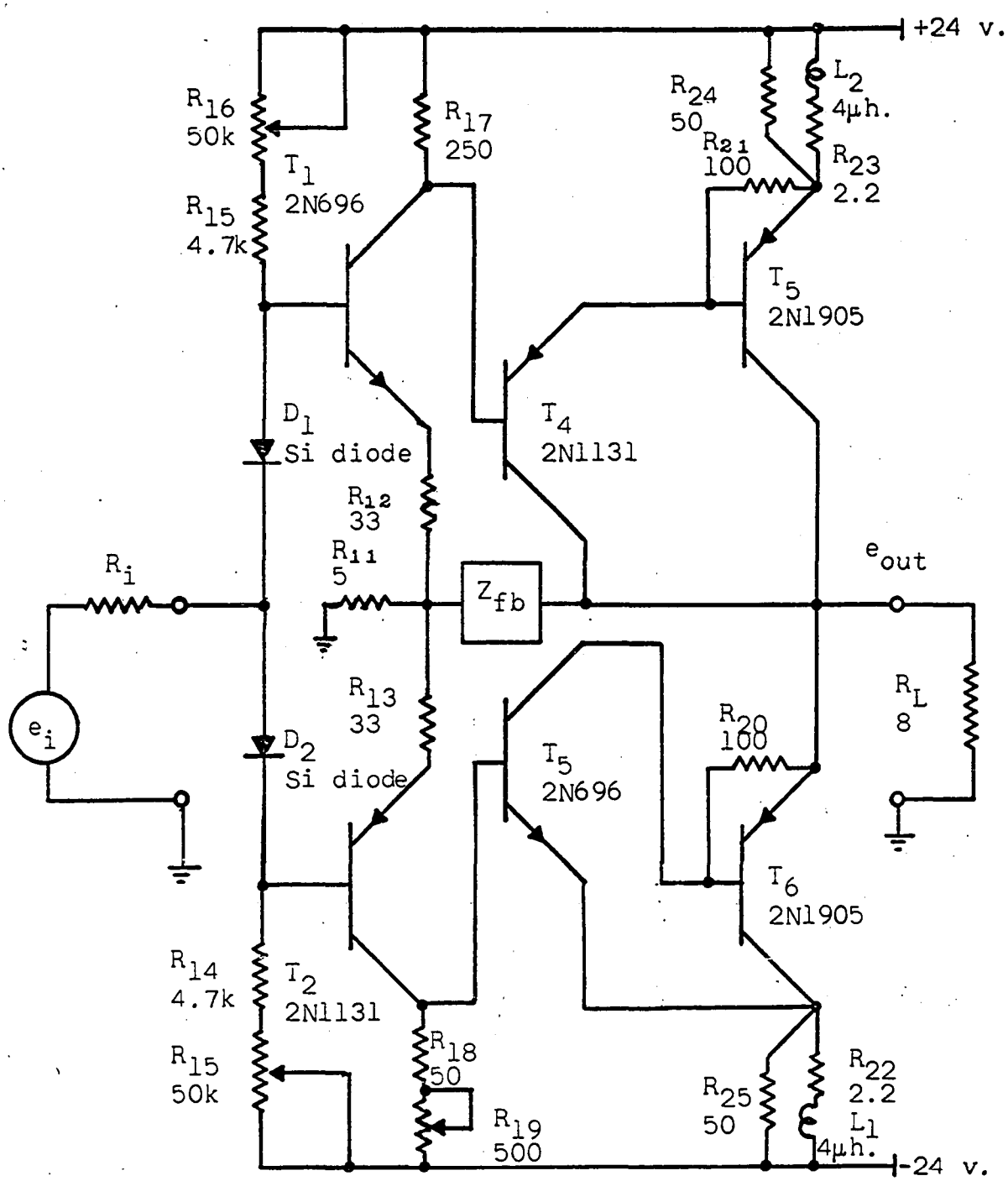
The final form of the output and driver stages is shown in Figure 9. Bias levels for both driver and output stages are conveniently controlled by the amount of forward bias on diodes D_1 and D_2. The resistance R_{18} - R_{19} is made variable so that minor mismatches in the current gains of T_1 and T_2 can be compensated. When either side of the amplifier is conducting, the circuit may be characterized by Figure 10a where T_1 or T_2 is represented by the z-parameter matrix,

$$[Z'] = \frac{1}{\frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu}} \begin{bmatrix} \frac{R'_x + Z'_\pi}{r'_o} + \frac{R'_x h'_{fe}}{Z'_\mu} & \frac{Z'_\pi}{Z'_\mu} \\ -h'_{fe} & 1 \end{bmatrix} \qquad (31)$$

and the composite transistor by the h-parameter matrix,

$$[H''] = \begin{bmatrix} R_1 & \varepsilon \\ \frac{R_1}{Z_3} & 0 \end{bmatrix} \quad \text{where } \varepsilon \text{ is a small non-zero constant.} \qquad (32)$$

While h''_{12} is essentially zero, it must be non-zero for the following analysis. Combining $[Z']$ and $[Z_f]$, Figure 10a



All resistances specified in ohms.
Z_{fb} consists of a 50 ohm resistor in parallel with a 0.01 microfarad capacitor.

Figure 9. The output and driver stages

becomes Figure 10b, where

$$[Z'''] = \frac{1}{\frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu}} \begin{bmatrix} \frac{R'_x + Z'_\pi + Z_f}{r'_o} + \frac{(R'_x + Z_f)h'_{fe}}{Z'_\mu} & \frac{Z'_\pi}{Z'_\mu} + Z_f\left[\frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu}\right] \\ -h'_{fe} & 1 \end{bmatrix} \tag{33}$$

or

$$[B'''] = \frac{1}{\frac{Z'_\pi}{Z'_\mu} + \frac{Z_f}{r'_o} + \frac{Z_f h'_{fe}}{Z'_\mu}} \begin{bmatrix} 1 & R'_x + Z'_\pi + (1+h'_{fe})Z_f \\ \frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu} & \frac{R'_x+Z'_\pi+R_f}{r'_o} + \frac{(R'_x+R_f)h'_{fe}}{Z'_\mu} \end{bmatrix} . \tag{34}$$

Figure 10b is the same as 10c to a very good approximation, and

$$[B''] = \begin{bmatrix} \frac{1}{\varepsilon} & \frac{R_1}{\varepsilon} \\ 0 & \frac{-R_1}{Z_3} \end{bmatrix} . \tag{35}$$

Combining $[B''']$ and $[B^{iv}]$, Figure 10c becomes Figure 10d, where

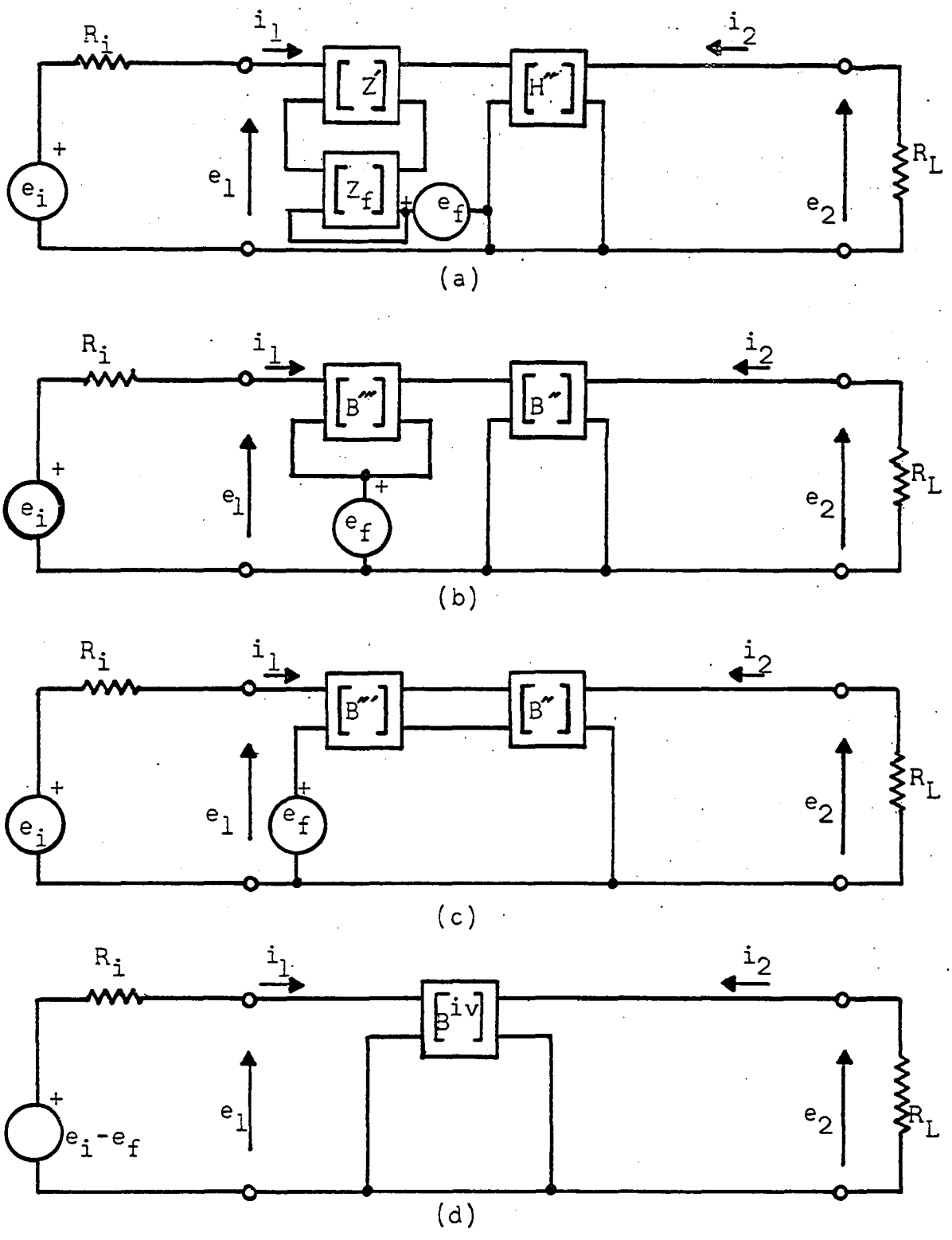


Figure 10. Sequence of two-port networks used in the analysis of the driver and output stages

$$[B^{iv}] = \frac{1}{\frac{Z'_\pi}{Z'_\mu} + \frac{Z_f}{r'_o} + \frac{Z_f h'_{fe}}{Z'_\mu}} \begin{bmatrix} \frac{1}{\varepsilon} + \frac{R_1}{\varepsilon}\left(\frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu}\right) & \\ & \\ -\frac{R_1}{Z_3}\left(\frac{1}{r'_o} + \frac{h'_{fe}}{Z'_\mu}\right) & \end{bmatrix}$$

$$\begin{pmatrix} \frac{1}{\varepsilon}\left(R'_x + Z'_\pi + (1+h'_{fe})Z_f\right) \\ +\frac{R_1}{\varepsilon}\left[\frac{R'_x + Z'_\pi + Z_f}{r'_o} + \frac{R'_x + Z_f h_{fe}}{Z'_\mu}\right] \end{pmatrix} \\ -\frac{R_1}{Z_3}\left[\frac{R'_x + Z'_\pi + Z_f}{r'_o} - \frac{(R'_x + Z_f)h_{fe}}{Z'_\mu}\right] \end{bmatrix} . \qquad (36)$$

Now

$$\begin{bmatrix} e_2 \\ i_2 \end{bmatrix} = [B^{iv}] \begin{bmatrix} e_1 \\ -i_1 \end{bmatrix}$$

$$\begin{bmatrix} e_2 \\ \frac{e_2}{R_L} \end{bmatrix} = [B^{iv}] \begin{bmatrix} e_1 \\ \frac{e_1 - (e_i - e_f)}{R_1} \end{bmatrix} \qquad (37)$$

and the solution to these equations is,

$$\frac{e_2}{e_i - e_f} = \frac{\Delta b^{iv}}{b_{22}^{iv} - \frac{b_{12}^{iv}}{R_L} + R_i\left(b_{21}^{iv} - \frac{b_{11}^{iv}}{R_L}\right)} \tag{38}$$

or

$$\frac{e_2}{e_i - e_f} = \frac{\frac{R_1}{Z_3} h_{fe}' R_L}{R_i + R_x' + Z_\pi' + (1+h_{fe}')Z_f} \quad . \tag{39}$$

It is possible to choose Z_f so that

$$(1 + h_{fe}')Z_f >> R_i + R_x' + Z_\pi' \tag{40}$$

in which case

$$\frac{e_2}{e_i - e_f} \approx \frac{R_1 R_L}{Z_3 Z_f} \quad . \tag{41}$$

It is desirable that the voltage gain be as high as possible, thus Z_f should be kept small, but a small Z_f makes the Inequality 40 a weak inequality. If Z_f is in the order of 40 ohms, Inequality 40 is an inequality of at least an order of magnitude and the low-frequency open-loop gain into an 8 ohm load is sufficiently high, i.e.,

$$\frac{e_2}{e_1 - e_f} = 114 \times \frac{8}{40} = 23 \quad . \tag{42}$$

The representation in Figure 10 may now be expressed in terms of the components in Figure 9.

$$e_f = \frac{e_{out} R_{11}}{R_{11} + Z_{fb}} \tag{43}$$

$$Z_f = R_{12} + \frac{R_{11}Z_{fb}}{R_{11} + Z_{fb}} \tag{44}$$

$$e_2 = e_{out} \cdot \tag{45}$$

With these substitutions, Equation 41 becomes,

$$\frac{e_{out}}{e_i} = \frac{\frac{R_1}{Z_3}\ \frac{R_L}{R_{12} + \frac{R_{11}\ Z_{fb}}{R_{11} + Z_{fb}}}}{1 + \frac{R_{11}\ R_1\ R_L}{Z_3(R_{12}R_{11} + R_{12}Z_{fb} + R_{11}Z_{fb})}} . \tag{46}$$

The impedance, Z_{fb}, determines the over-all transfer function of the driver-output stage. An easily implemented form of Z_{fb} is

$$Z_{fb} = \frac{R_{fb}}{1 + j\frac{f}{f_{fb}}} \tag{47}$$

and this results in a desirable over-all transfer function. Using Equation 29 for Z_3, Equation 46 becomes

$$\frac{e_{out}}{e_i} = \frac{1 + \frac{R_{fb}}{R_{11}(1 + j\ f/f_{fb})}}{\frac{[R_{12}R_{11} + (R_{12} + R_{11})\frac{R_{fb}}{1+j\ f/f_{fb}}]R_3(1+j\ \frac{f}{f_3})}{R_{11}\ R_1\ R_L} + 1} . \tag{48}$$

The inequality,

$$\left| R_{12}\left(1 + j\frac{f}{f_3}\right)\right| < \left| \frac{(R_{12} + R_{11})R_{fb}}{R_{11}} \right| \qquad (49)$$

is valid to about 3 megacycles for the component values used in the final design and provides an approximation which greatly simplifies the remaining algebra. With this approximation, Equation 48 becomes,

$$\frac{e_{out}}{e_{in}} = \frac{(R_{fb} + R_{11})R_1R_L}{(R_{12} + R_{11})R_{fb}R_3 + R_1R_{11}R_L} \cdot \frac{1 + j\dfrac{f}{\dfrac{R_{11}+R_{fb}}{R_{11}}\, f_{fb}}}{1 + j\dfrac{f}{\dfrac{[(R_{12}+R_{11})R_{fb}R_3 + R_1R_{11}R_L]f_3f_{fb}}{(R_{11} + R_{12})R_{fb}R_3f_{fb} + R_{11}R_1R_Lf_3}}} \qquad (50)$$

That the driver and output stages form a feedback amplifier is evident from the above analysis. Thus the analysis is valid only if the system is stable. Standard procedures are available for determining the stability of such a system and such a stability analysis limits the useful range of values which may be chosen for the various components. The process of selection of components is a trial and error process and will not be described here, but it may be verified, if desired, that the component values selected do satisfy the stability requirements with a reasonable margin of safety. The remaining

components to be selected and their selected values are:

$$R_{11} = 5 \text{ ohms}$$

$$R_{12} = R_{13} = 33 \text{ ohms}$$

$$R_{fb} = 50 \text{ ohms}$$

$$C_{fb} = 0.01 \text{ microfarad.}$$

This results in a feedback-impedance breakpoint of

$$f_{fb} = \frac{1}{2\pi \times 50 \times 10^{-8}} \approx 3 \times 10^{-5} \text{ cps} \tag{51}$$

and Equation 50 becomes,

$$\frac{e_{out}}{e_{in}} = 7.54 \; \frac{1 + j \dfrac{f}{3.3 \times 10^{6}}}{1 + j \dfrac{f}{1.94 \times 10^{5}}} \tag{52}$$

which is the voltage transfer function of the driver-output stages.

Distortion of the Driver-Output Stages

The reduction in low-frequency harmonic distortion in a feedback amplifier is given by (11):

$$d_{cl} = \frac{d_{ol}}{1 + GH} \tag{53}$$

where

d_{cl} = closed loop distortion

d_{ol} = open loop distortion

GH = low frequency loop gain

thus the maximum distortion of the driver and output stages is,

$$d = \frac{8.8}{3.1} \approx 2.8\% \tag{54}$$

where $1 + GH = 3.1$ is determined from Equation 42 and Equation 52. Actual measurement indicates that d is less than 2%.

THE COMPLETE AMPLIFIER

The development of the output and driver stages for an amplifier of extraordinary capability is described in the previous chapters. In order to demonstrate this capability, it is necessary to design a complete amplifier whose specifications are considerably better than the amplifiers which are currently available. Here it should be recognized that the choice of specifications is to a great extent arbitrary and would ordinarily be determined by the application. However, since no particular application is intended, it was decided that wide bandwidth and low distortion should be the principal criteria used to determine the desired specifications. Specifically, it was decided that the amplifier should have as wide a bandwidth as possible consistent with the requirement that the maximum harmonic distortion in the output be about an order of magnitude below the harmonic distortion of presently available amplifiers (i.e., about an order of magnitude below 0.1%). These specifications are to be met while delivering reasonable power levels to an 8 ohm resistive load.

Since the distortion products are in the order of 2% in the output and driver stages, it will be necessary that the total feedback around these stages be in the order of 46 db in order to reduce the distortion products by a factor of 1/200 to a desired value of about 0.01%. There are several reasons why it is undesirable to attempt this much feedback

in a single feedback loop. First, it would require the design of a broadband direct-coupled amplifier with a gain greater than 200 with negligible drift. Second, it would require that at least the upper two decades of the amplifier pass band be involved in the stabilization of the feedback loops. Third, the compensation problems would be complicated by the fact that the compensation would have to take into account the pole in the driver-output transfer function as well as the poles and zeros of the compensation network. The necessary 46 db of feedback can be achieved quite conveniently through the use of two feedback loops of approximately 23 db each as is indicated in block diagram form in Figure 11. The block represented by

$$G_1 = \frac{7.54\ (1 + j\ \frac{f}{3.3 \times 10^6})}{1 + j\ \frac{f}{1.94 \times 10^5}}$$

is the transfer function of the driver-output combination. The problem is to find G_2, H_2, G_3 and H_3 such that

$$G_1G_2G_3H_3\Big|_{\text{low frequency}} = 200$$

and such that maximum bandwidth is achieved with stable feedback. Stability is the major factor in determining the characteristics of the feedback loops. However, stability analysis is well documented in any of the standard texts on feedback systems (2). Thus the details of the design procedure

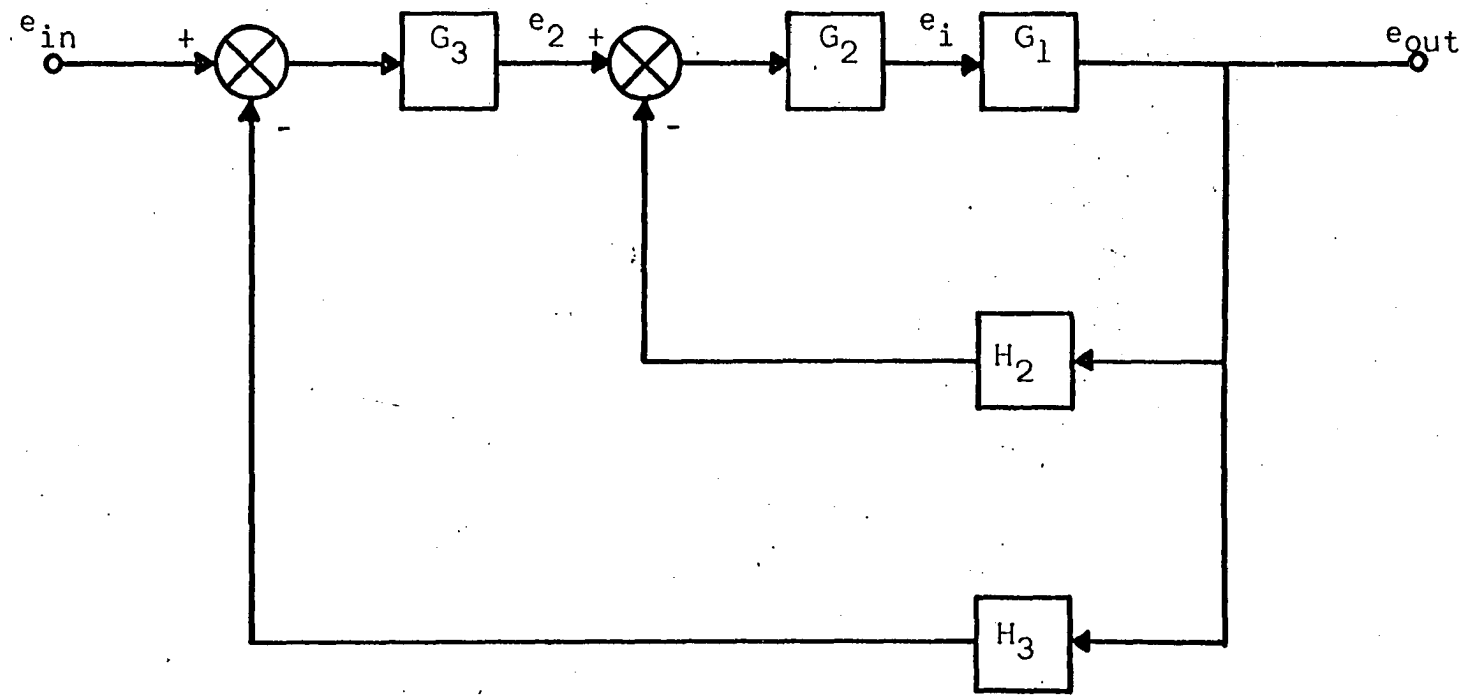


Figure 11. Block diagram of the complete amplifier

will not be discussed in full. The choice of G_2 and H_2 is made so that the transfer function e_{out}/e_2 is maximally flat consistent with stability and gain requirements. This can be accomplished by choosing

$$G_2 = 12$$

and

$$H_2 = 0.0836$$

so that the over-all transfer function is

$$\frac{e_{out}}{e_2} = \frac{G_1 G_2}{1 + G_1 G_2 H_2}$$

$$= \frac{90.5 \; 1 + j \dfrac{f}{3.3 \times 10^6}}{1 + 7.55 \; 1 + j \dfrac{f}{3.3 \times 10^6}} \Big/ \frac{1 + j \dfrac{f}{1.94 \times 10^5}}{1 + j \dfrac{f}{1.94 \times 10^5}}$$

$$= \frac{10.6 \left(1 + j \dfrac{f}{3.3 \times 10^6}\right)}{1 + j \dfrac{f}{1.33 \times 10^6}} . \qquad (55)$$

The transfer functions G_2 and H_2 are implemented by the amplifier shown in Figure 12. Analysis of this amplifier can be accomplished by standard techniques and such analysis will show that the above transfer functions are satisfactorily approximated by the amplifier. The choice of

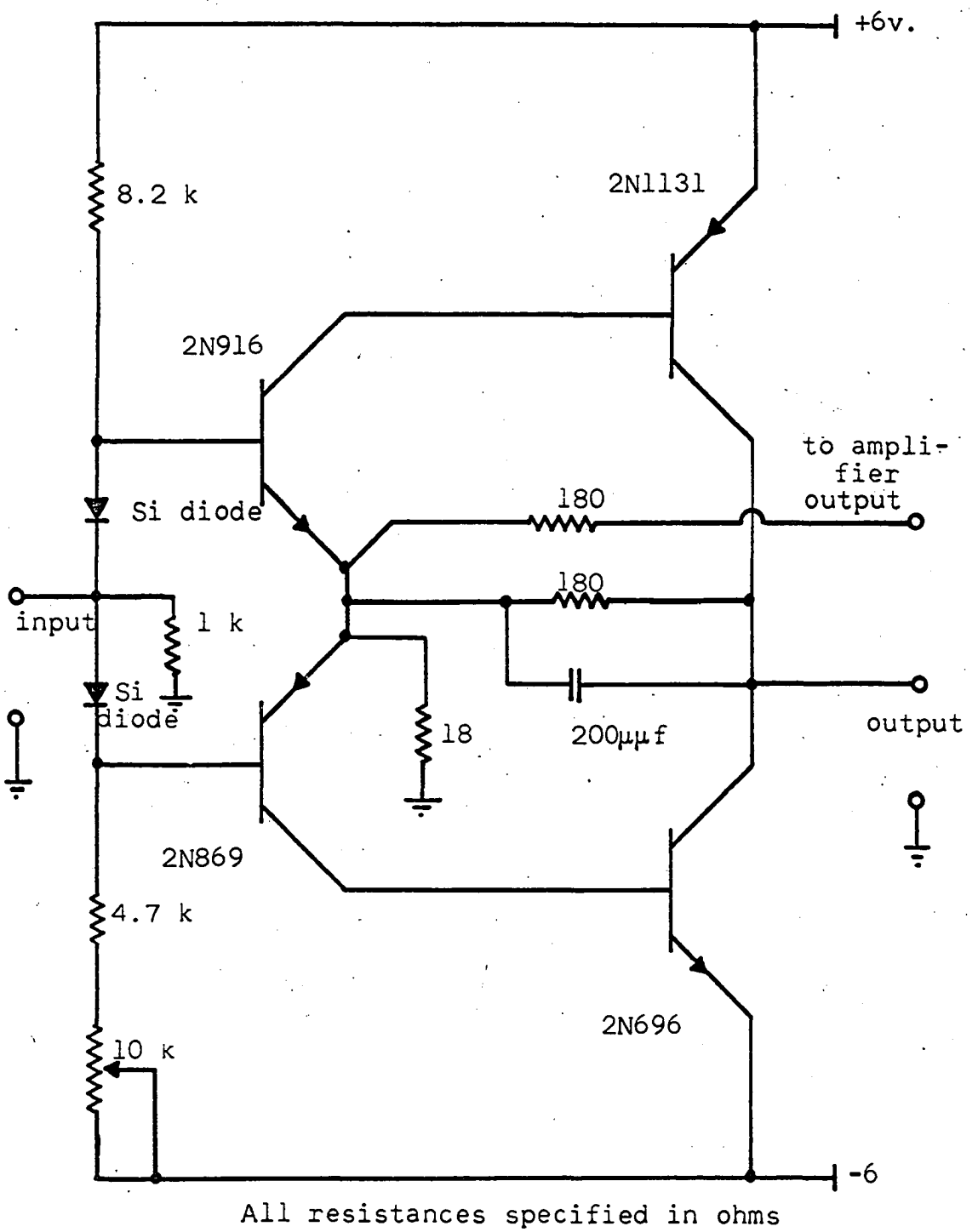


Figure 12. Amplifier for the implementation of G_2 and H_2

$$G_3 = \frac{37.5\ (1 + j\ \frac{f}{150{,}000})}{1 + j\ \frac{f}{4{,}000}}$$

and

$$H_3 = \frac{0.089}{1 + j\ \frac{f}{168{,}000}}$$

results in an over-all transfer function,

$$\frac{e_{out}}{e_{in}} = \frac{400\ \dfrac{(1 + j\ \frac{f}{0.15 \times 10^6})(1 + j\ \frac{f}{3.3 \times 10^6})}{(1 + j\ \frac{f}{0.004 \times 10^6})(1 + j\ \frac{f}{1.33 \times 10^6})}}{1 + 35.6\ \dfrac{(1 + j\ \frac{f}{0.15 \times 10^6})(1 + j\ \frac{f}{3.3 \times 10^6})}{(1 + j\ \frac{f}{0.004 \times 10^6})(1 + j\frac{f}{1.33 \times 10^6})(1 + j\frac{f}{0.168 \times 10^6})}}$$

$$= \frac{10.9\ (1 + j\ \frac{f}{0.15 \times 10^6})(1 + j\ \frac{f}{3.3 \times 10^6})(1 + j\frac{f}{0.168 \times 10^6})}{(1 + j\frac{f}{1.22 \times 10^6})(1 + j\ \frac{f}{0.238 \times 10^6})(1 + j\ \frac{f}{0.114 \times 10^6})} \qquad (56)$$

which deviates from the low-frequency gain of 10.9 by less than 1 db to a frequency greater than 1 megacycle. The transfer functions G_3 and H_3 are implemented by the amplifier shown in Figure 13.

The voltage-gain and phase-response characteristics of the complete amplifier driving an 8 ohm load are shown in Figure 14. An asymptotic plot of Equation 56 also shown in Figure 14,

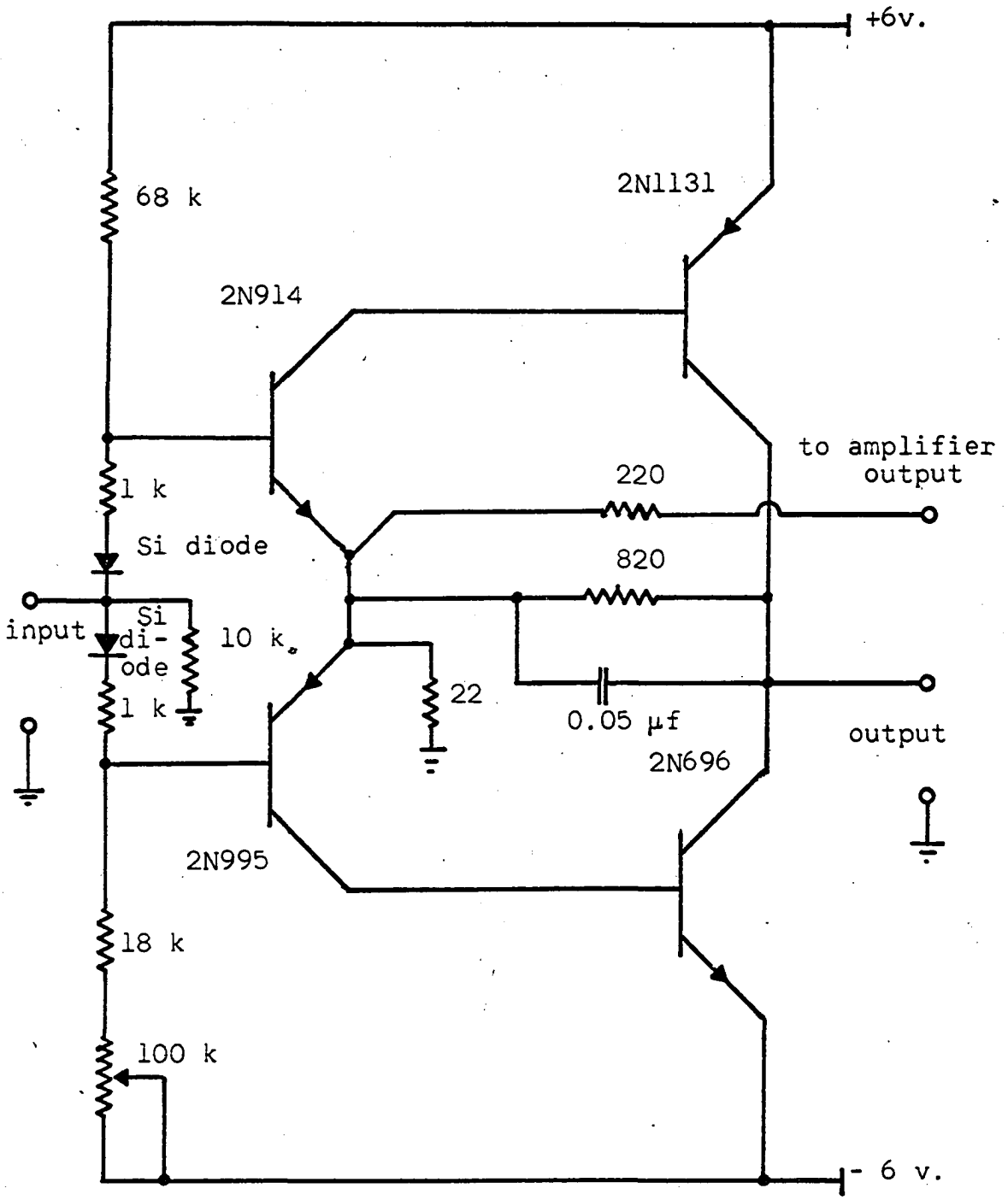


Figure 13. Amplifier for the implementation of G_3 and H_3

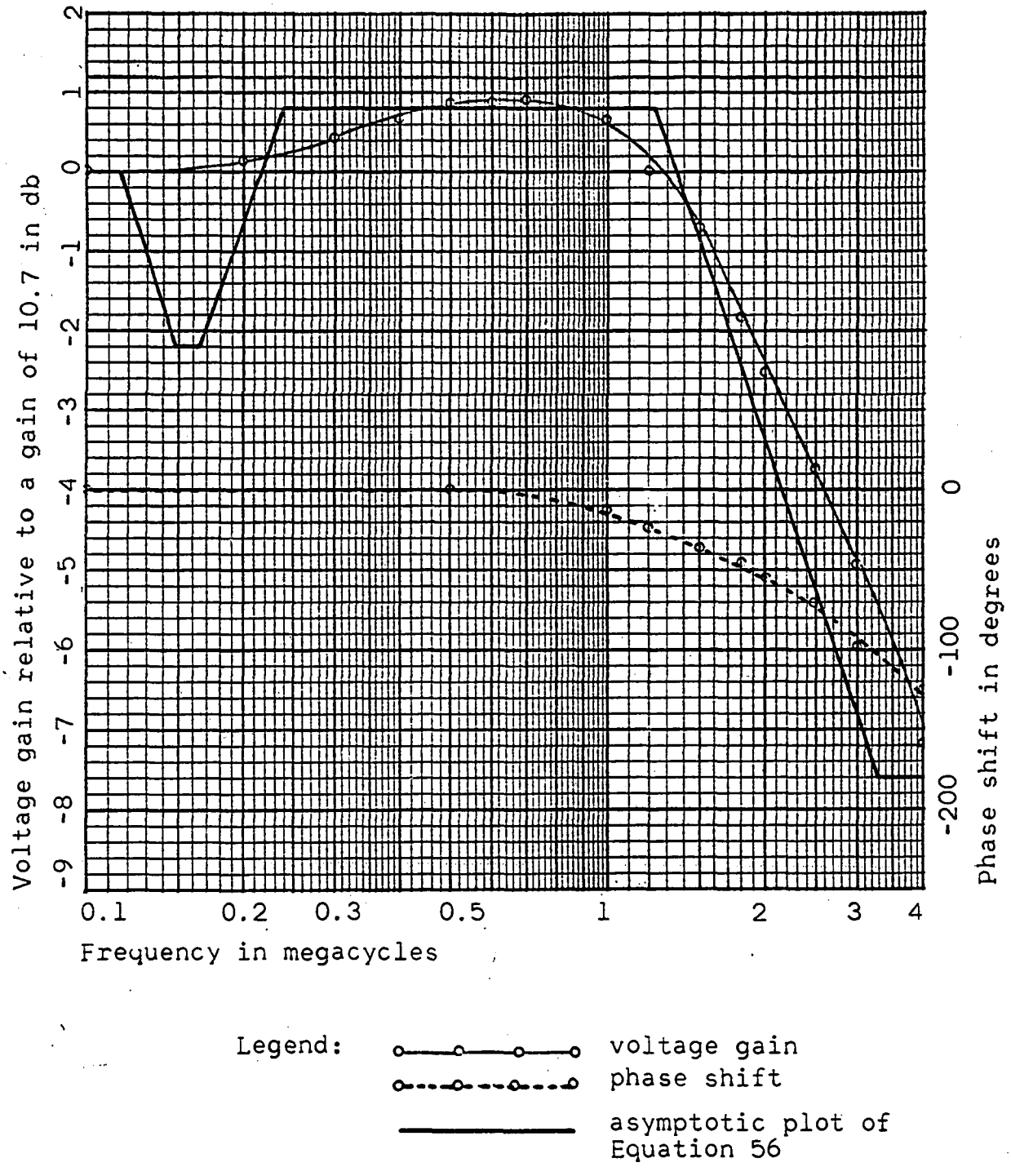


Figure 14. Response characteristics of the amplifier driving an 8 ohm load

demonstrates the validity of the previous analysis. The voltage-gain and phase-response characteristics of the complete amplifier with the output open circuited are shown in Figure 15. The similarity of these characteristics to those of the loaded amplifier demonstrates the ability of the amplifier to adapt to various loads while maintaining excellent response characteristics. Figure 16, the response of the amplifier to a 200 kc. square wave, demonstrates the excellent transient characteristics of the amplifier.

Distortion

The low-frequency distortion is approximately reduced by the factor, $G_1G_2G_3H_3|_{\text{low-frequency}}$, which in this case is

$$G_1G_2G_3H_3|_{\text{low-frequency}} = 7.54 \times 12 \times 37.5 \times 0.089$$

$$= 303$$

and the low frequency distortion should be in the order of

$$d_{amp} = d/G_1G_2G_3H_3|_{\text{low-frequency}} = 2\%/303 = 0.007\% .$$

Distortion of this order is very difficult to measure experimentally but the complete absence of phase shift at the low frequencies permits the use of techniques which are not applicable to ordinary amplifiers. If there is no appreciable phase shift in the amplifier, the circuit of Figure 17 may be used to measure the distortion. If R_2 is adjusted properly (i.e., for minimum reading in the VTVM #1) then the amplified

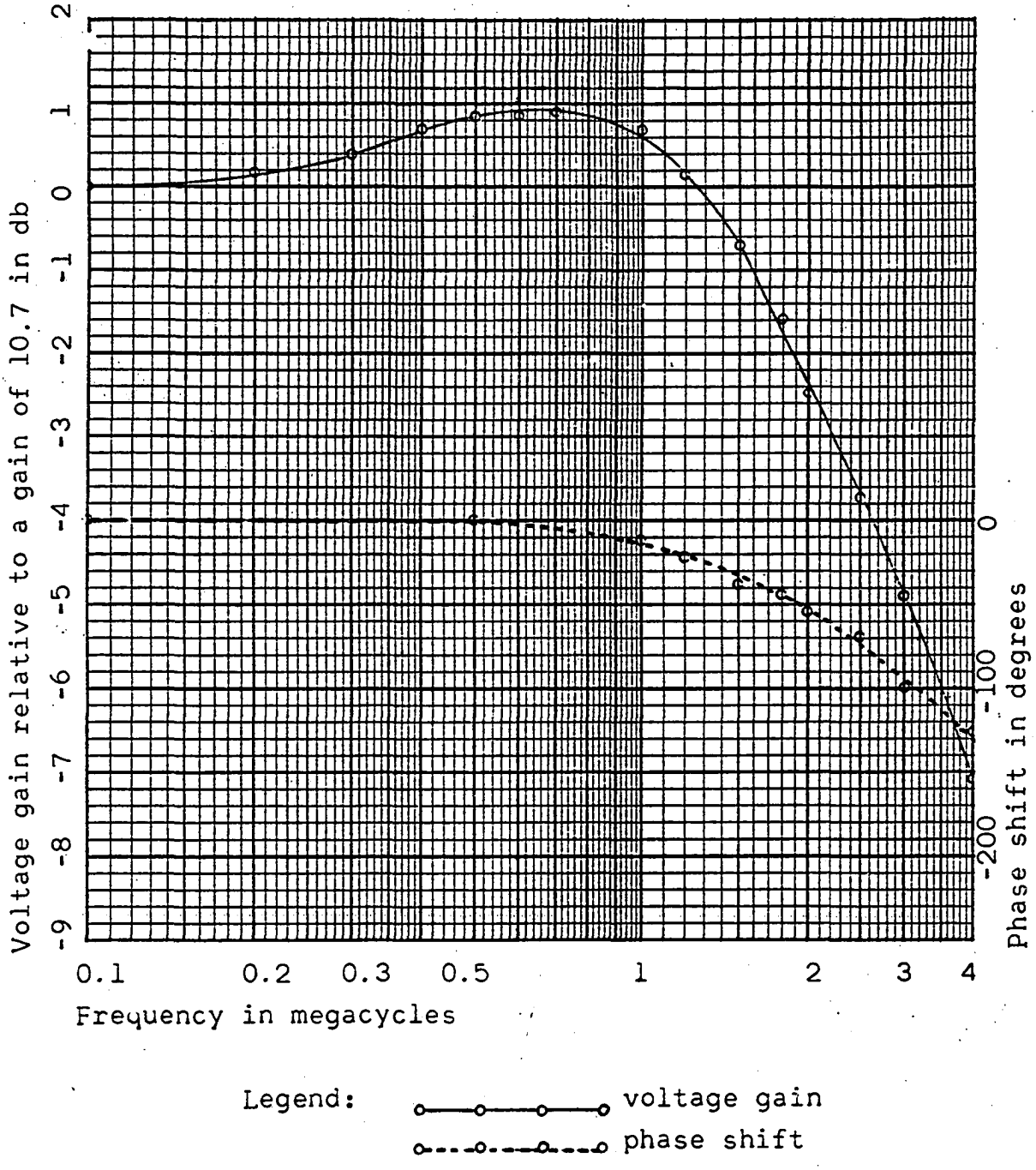
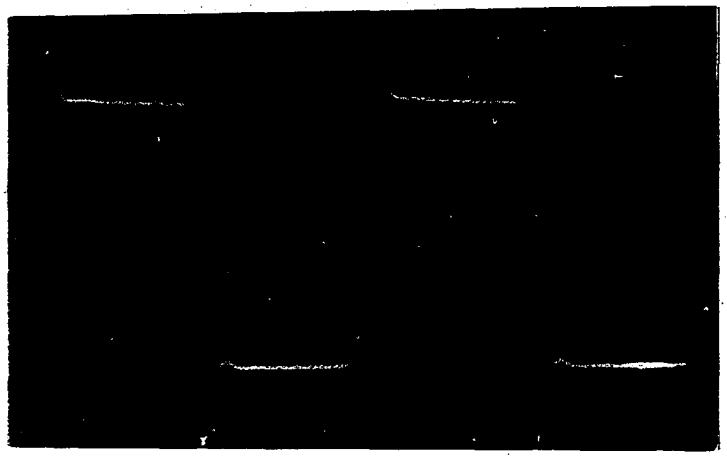


Figure 15. Response characteristics of the amplifier with the output open circuited

Vertical sensitivity = 0.2 volt/division
Sweep rate = 1 microsecond/division

Figure 16a. Response of the amplifier to a 200 kc. square wave when driving an 8 ohm load



Vertical sensitivity = 0.2 volt/division
Sweep rate = 1 microsecond/division

Figure 16b. Response of the amplifier to a 200 kc. square wave when open circuited

components of e_{in} exactly cancel the voltage e_g and the VTVM #1 will read only the distortion products in the output. With an 8 ohm load the following data was taken at 100 cps:

e_{out} volts	power watts	$e_{VTVM\ \#1}$ millivolts	distortion per cent
10	12.5	1.8	0.018
11	15	6	0.05
11.5	16.5	28	0.24

At least 0.5 millivolts of noise and hum pickup was unavoidable. The impossibility of securing a perfect balance in the circuit also contributed to a higher reading on the VTVM #1 than the actual distortion products. Thus the actual distortion should be less than that measured by this method.

Input and Output Impedance

The input impedance is determined almost entirely by the resistances in parallel with the input terminals. The measured value of the input resistance was 7,000 ohms.

The output impedance was measured by applying a 0.3 ampere, 1000 cps current to the output terminals with the input terminals grounded. A 3 millivolt signal was observed at the output. The output impedance at 1000 cps determined from this data was

$$Z_{out} = 0.003/0.3 = 0.01 \text{ ohm}$$

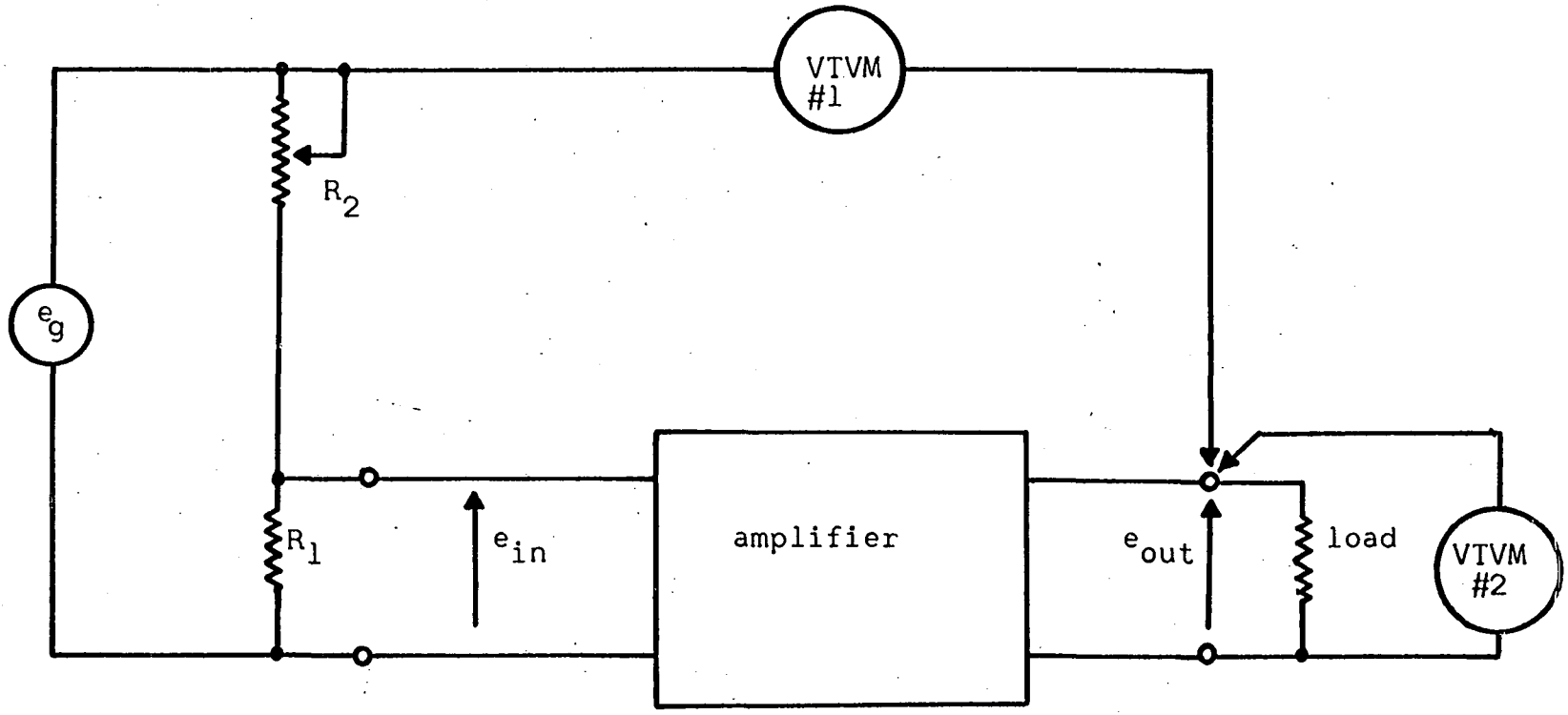


Figure 17. Circuit for measuring distortion

Power Output

The maximum low-frequency power delivered to the load is entirely a function of the saturation resistance of the composite transistors, the supply voltage, and the load resistance. There is no need to be concerned about the collector dissipation in establishing the maximum-power rating since all transistors are operating well within this rating if an adequate heat sink is provided. Using typical values, the peak voltage in the output waveform is,

$$V_{load} = \frac{V_{supply}\ R_L}{R_{sat} + R_L} = \frac{24 \times 8}{3.2 + 8} = 17.2 \text{ volts}$$

which, for a sine-wave output, corresponds to a maximum power output of

$$P_{max} = 17.2^2/2 \times 8 = 18.7 \text{ watts.}$$

This is somewhat greater than the maximum power output indicated by the distortion measurements, but variations in power-supply voltage could easily account for this difference.

After the sad experience of several power transistor failures, it was discovered that another mechanism besides collector dissipation must cause these transistors to fail at the higher frequencies. Several units failed when an attempt was made to secure more than 5-10 watts of power at frequencies of 100 kc. and above. It is believed that there are no mechanisms of transistor failure described in the literature

which will account for this behavior. The matter was not further investigated due to the expense of transistor replacement.

SUMMARY AND CONCLUSIONS

The literature reveals that the complementary-symmetry circuits proposed by Sziklai a decade ago have not been used to great advantage in spite of their great potential. The principle reason for this is that suitable enantiomorphic transistors are not available. For transistors to be suitable in this application, they must be available in both polarities, must be capable of dissipating a considerable amount of power, must have linear and matched current transfer characteristics, and must have high frequency characteristics which are well matched. It has been demonstrated that it is possible to design composite transistors which are extremely well suited to application in complementary-symmetry circuits. These composite transistors have an extremely linear current transfer characteristic which is adjustable so that two complementary transistors can be matched. They can be made with either polarity but the transistor which dissipates a large percentage of the power can be of the same polarity in either case. The composite transistors also have well-matched and controlled high-frequency characteristics.

It appears that the composite transistors can be used to advantage in a number of different circuits. Their unique characteristics are demonstrated in a linear amplifier. The fact that enantiomorphic pairs are available enables one to direct-couple the amplifier to the load. Low distortion,

particularly second harmonic, is a result of one's ability to match composite transistors of opposite polarity. The fact that the high-frequency characteristics are well matched and controlled enables one to design feedback networks with the assurance that such things as the multiple resonances in output transformers will not cause the system to be unstable. The amplifier which was designed to demonstrate these principles had a frequency response from d-c to 2 megacycles. A novel method of distortion measurement was developed to verify that the distortion of the amplifier was less than 0.02%. Both of these figures demonstrate performance significantly better than the performance of currently available amplifiers.

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APPENDIX

Evaluation of H-Parameters from the Hybrid-π Model

The standard hybrid-π model for the common-emitter configuration is shown in Figure 18a. This may be redrawn as shown in Figure 18b. Since

$$V = \frac{V_o \; Z_\pi}{Z_\mu + Z_\pi} + \frac{I_i \; Z_\pi \; Z_\mu}{Z_\pi + Z_\mu}$$

and

$$I_o = g_m V + V_o / r_o$$

$$= \frac{Z_\pi \; Z_\mu}{Z_\pi + Z_\mu} \; g_m I_i + \left[\frac{1}{r_o} + \frac{Z_\pi g_m}{Z_\mu + Z_\pi} \right] V_o$$

these expressions may be used to convert the circuit of Figure 18b to that of Figure 18c, which is the standard circuit representing the h-parameter notation. The h-parameters are easily identified from this circuit. The expression for the exact h-parameters along with their approximations are,

$$h_{11} = R_x + \frac{Z_\pi \; Z_\mu}{Z_\pi + Z_\mu} \approx R_x + Z_\pi$$

$$h_{12} = \frac{Z_\pi}{Z_\mu + Z_\pi} \approx \frac{Z_\pi}{Z_\mu}$$

$$h_{21} = \frac{Z_\pi \; Z_\mu \; g_m}{Z_\mu + Z_\pi} \approx Z_\pi g_m = h_{fe}$$

$$h_{22} = \frac{1}{r_o} + \frac{Z_\pi \; g_m}{Z_\mu + Z_\pi} \approx \frac{1}{r_o} + \frac{h_{fe}}{Z_\mu} \; .$$

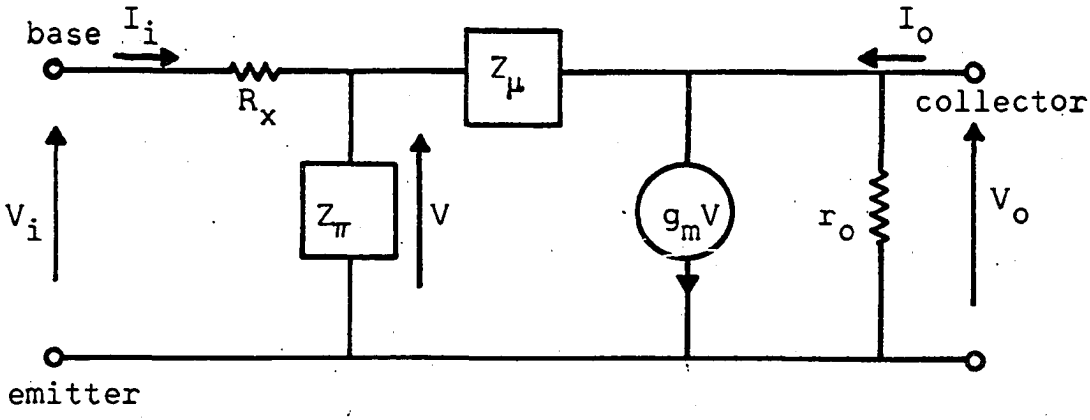

Figure 18a. Hybrid-π model of a transistor

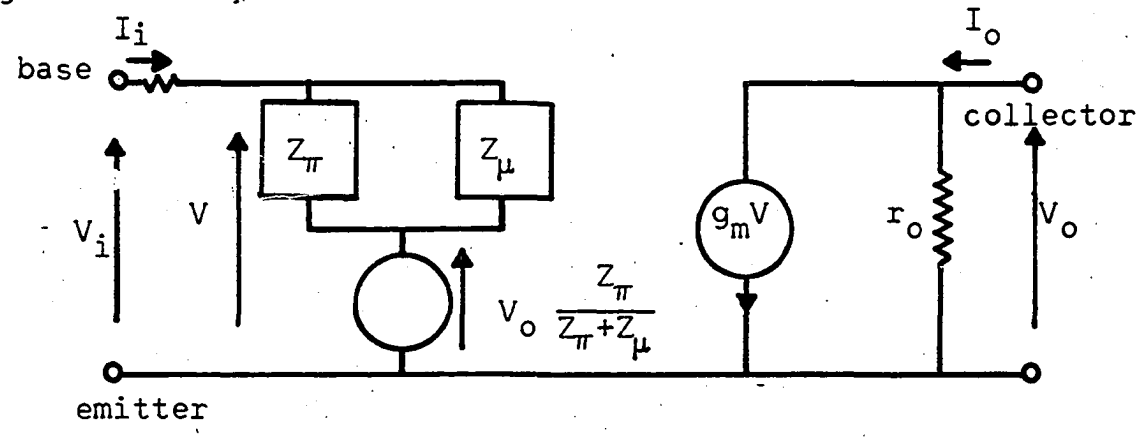

Figure 18b. A modified form of the hybrid-π model

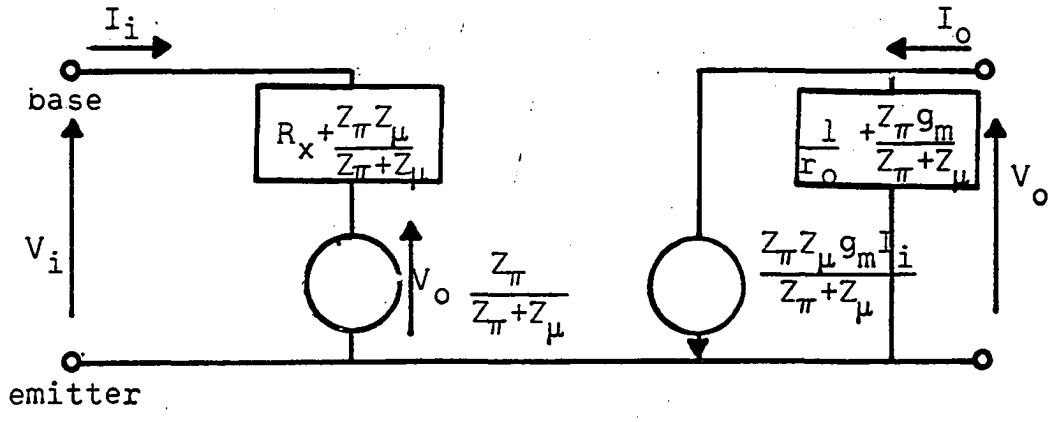

Figure 18c. The hybrid-π model in h-parameter form

The determinant of the approximate h-parameters is

$$\Delta^h = (R_x + Z_\pi)\left[\frac{1}{r_o} + \frac{h_{fe}}{Z_\mu}\right] - \frac{Z_\pi h_{fe}}{Z_\mu}$$

$$= \frac{R_x + Z_\pi}{r_o} + \frac{R_x h_{fe}}{Z_\mu} .$$

The h-parameters of the common-collector arrangement are also required. The relationships

$$h_{ic} = h_{ie}$$

$$h_{rc} = 1 - h_{re}$$

$$h_{fc} = -(1 + h_{fe})$$

$$h_{oc} = h_{oe}$$

may be used to derive the common-collector h-parameters from the above common-emitter h-parameters. Thus, for the common-collector configuration,

$$h_{11} = R_x + \frac{Z_\pi Z_\mu}{Z_\pi + Z_\mu} \approx R_x + Z_\pi$$

$$h_{12} = 1 - \frac{Z_\pi}{Z_\mu + Z_\pi} = \frac{Z_\mu}{Z_\mu + Z_\pi} \approx 1$$

$$h_{21} = -\left(1 + \frac{Z_\pi Z_\mu g_m}{Z_\mu + Z_\pi}\right) = -(1 + h_{fe})$$

$$h_{22} = \frac{1}{r_o} + \frac{Z_\pi g_m}{Z_\mu + Z_\pi} \approx \frac{1}{r_o} + \frac{h_{fe}}{Z_\mu} .$$

The determinant of the common-collector h-parameters is

$$\Delta^h = (R_x + Z_\pi)\left(\frac{1}{r_o} + \frac{h_{fe}}{Z_\mu}\right) + 1 + h_{fe}$$

$$\simeq 1 + h_{fe} .$$

In most of the equations relating these parameters it is necessary to make simplifying approximations. These approximations are based on the inequality

$$r_x + Z_\pi << r_o << Z_\mu$$

which is valid for all typical transistors. The inequalities are typically inequalities of 2 orders of magnitude for good transistors at low frequency but the last inequality becomes weaker as the frequency is increased beyond the breakpoint frequency of the Z_μ impedance.